	Scenario A	Scenario B	Scenario C
Luminosity (10^{32}cm^{-1}s^{-1})	< 1	1 - 2	1 - 2
Beam crossing interval (ns)	396	132	396
$p_T^{(1)}$, $p_T^{(2)}$ (GeV/c)	> 2	> 2.25	> 2.5
$p_T^{(1)} + p_T^{(2)}$ (GeV/c)	> 5.5	> 6	> 6.5
$\Delta\phi$	$< 135°$	$< 135°$	$< 135°$
Cross section (μb)	252 ± 18	152 ± 14	163 ± 16

Table 2.15: Level-1 XFT trigger cuts and cross sections for the three Tevatron operating scenarios considered.

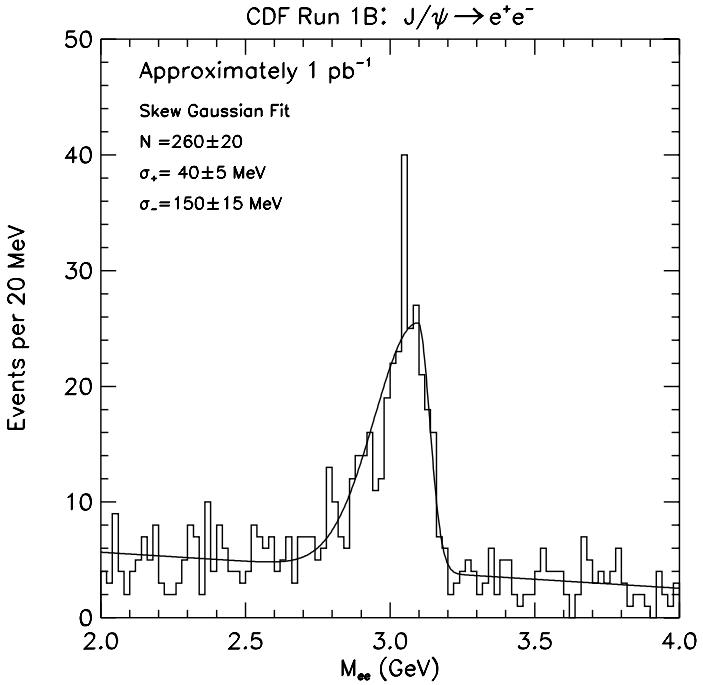

Figure 2.64: $J/\psi \to e^+e^-$ signal from a test trigger during Run I.

2.7.5.2 *CP* Asymmetry in $B_s^0 \to J/\psi\,\phi$

While the *CP* asymmetry in $B^0 \to J/\psi K_S$ measures the weak phase of the CKM matrix element V_{td} in the standard convention, the *CP* asymmetry in $B_s^0 \to J/\psi\,\phi$ measures the weak phase of the CKM matrix element V_{ts}. The latter asymmetry is expected to be very small in the Standard Model, but in the context of testing the Standard Model has the same fundamental importance as measuring the more familiar *CP* asymmetries. This measurement is most accessible, if not unique, to experiments at a hadron collider.

Our Run I B_s^0 mass analysis indicates that our yield of reconstructed $B_s^0 \to J/\psi\,\phi$ events is 40% that of $B^0 \to J/\psi K_S$ (see Figure 2.65). Since the improvements for $B^0 \to J/\psi K_S$ ($\approx 20,000$ dimuon events) apply equally to $B_s^0 \to J/\psi\,\phi$, we can expect ≈ 8000 events for this decay mode in Run IIa.

The flavor tagging techniques for the B_s^0 are the same as those for the B^0, with one exception: The fragmentation track correlated with the B_s^0 meson is a kaon instead of a pion. A PYTHIA study indicates that the Time–of–Flight system, by identifying kaons, will allow us to increase the efficiency of the same-side kaon algorithm from 1.0% to 4.2% [19]. Thus, we assume a total flavor tagging efficiency (ϵD^2) for B_s^0 mesons of 11.3%

The magnitude of a *CP* asymmetry in $B_s^0 \to J/\psi\,\phi$ decays will be modulated by the frequency of B_s^0 oscillations. Thus, for a meaningful limit, we must be able to resolve B_s^0 oscillations. If we neglect ($c\tau$) resolution effects and scale from the $B^0 \to J/\psi K_s$ mode, we can expect a precision on the asymmetry of ± 0.07 from a time dependent measurement in Run IIa. However, resolution effects smear the oscillations and produce

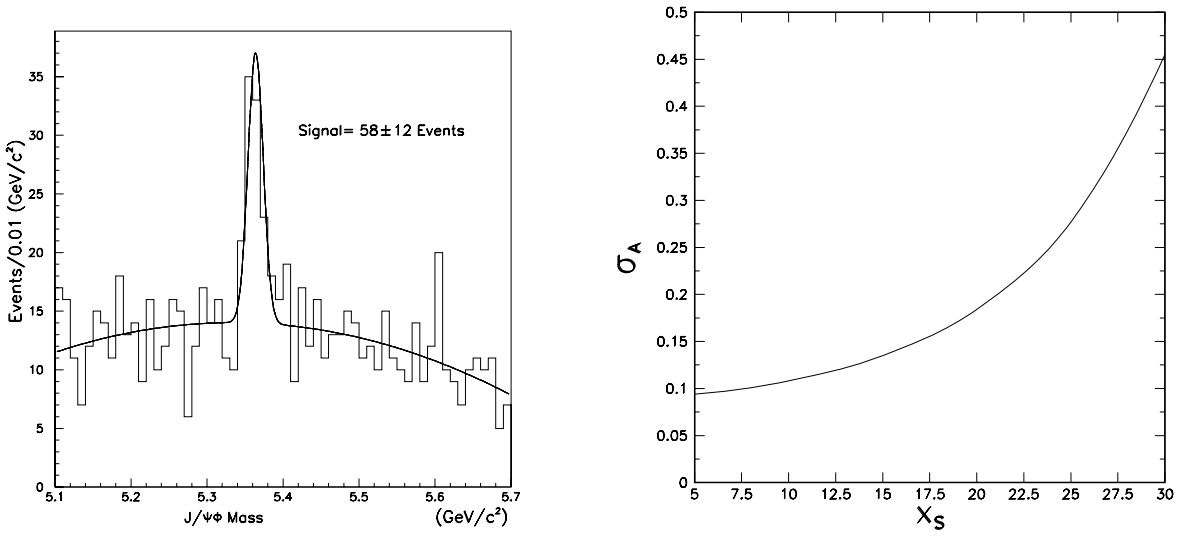

Figure 2.65: Left: The reconstructed mass distribution for $B_s^0 \to J/\psi\,\phi$ decays. SVX track information has been required for the muons from the J/ψ. Right: The uncertainty on the *CP* asymmetry for $B_s^0 \to J/\psi\,\phi$ as a function of the B_s^0 mixing parameter x_s.

an additional dilution factor of

$$D_{res} = e^{\left(\frac{-x_s^2\sigma_\tau^2}{2\tau^2}\right)}, \qquad (2.8)$$

where $x_s = \Delta m_s/\Gamma_s$, σ_τ is the resolution on the proper decay time, and τ is the average B_s^0 lifetime. With the addition of Layer 00, we expect that the proper lifetime resolution for the SVX II will be $\sigma_\tau/\tau \approx 0.03$ [20]. For $x_s = 25$, this dilution degrades the resolution on the asymmetry by a factor of 1.3.

There is an additional complication in this mode if the $J/\psi\,\phi$ final state is not a *CP* eigenstate. If this mode were a *CP* eigenstate, then the full resolution on the *CP* asymmetry would apply. If the mode is a mixture of *CP* states, then an angular fit including the *CP* violation is needed. Studies indicate that if this mode is an equal mixture of *CP*-even and *CP*-odd states, then the resolution on the *CP* asymmetry as determined from the angular fit is degraded by a factor of roughly 2. In Run I, CDF measured the *CP* even fraction to be 0.77 ± 0.19 [8].

With 15 fb^{-1} of data in Run 2b, $x_s = 25$, and vertex resolution comparable to Run IIa, we expect to measure the *CP* asymmetry in $B_s^0 \to J/\psi\,\phi$ with a resolution between 0.03 and 0.06, depending on the *CP* content of the final state. This is close to the Standard Model expectation of roughly 0.02, making us quite sensitive to new *CP*-violating physics in this mode.

2.7.5.3 *CP* Asymmetry in $B_s^0 \to J/\psi\eta^{(\prime)}$

Measuring the *CP* asymmetry in $B_s^0 \to J/\psi\eta^{(\prime)}$ decays is very similar to measuring it in $B_s^0 \to J/\psi\,\phi$, with two notable exceptions. First, the $J/\psi\eta$ and $J/\psi\eta'$ final states are *CP* eigenstates, so no angular fit is required and hence there is no degradation.

Second, the presence of photons in the final state (we detect the $\eta^{(\prime)}$ via its $\gamma\gamma$ decay mode) make these modes much more difficult for CDF. The CDF calorimeter was not designed to detect and measure low energy photon with very good energy resolution. However, CDF is capable of detecting these signals. Figure 2.66 shows the invariant mass of diphotons selected from our inclusive electron trigger data, which represent a data sample enhanced in $b\bar{b}$ events. Photon candidates were required to be in separate calorimeter towers, have $E_T^\gamma > 1$ GeV/c^2, and satisfy

requirements on E_{had}/E_{EM}, isolation, and pulse in the strip chambers. Clear π^0 and η signals can be seen.

The resolution on the reconstructed B_s^0 mass can be improved by constraining the photons to the η or η' mass. Monte Carlo studies show that the B_s^0 mass resolution will be better than 40 MeV/c^2, which is more than a factor of two worse than our mass resolution in all charged track decays but still should be more than sufficient to observe this mode.

Scaling from the expected number of $B^+ \to J/\psi K^+$ events, the ratio of B^0 to B_s^0 production, and the expected relative branching ratios, we expect 8000 $B_s^0 \to J/\psi\eta$ events in Run IIb[9]. Studies of J/ψ events in Run I indicate that with a 40 MeV/c^2 mass resolution, the background to signal ratio should be no more than 2. Using $x_s = 25$ and a proper time resolution of $\sigma_\tau/\tau = 0.03$, we expect to measure the *CP* asymmetry in this mode with a resolution of 0.11.

2.7.5.4 *CP* Asymmetry in $B^0 \to \pi^+\pi^-$ and $B_s^0 \to K^+K^-$

The *CP* asymmetry in the decay $B^0 \to \pi^+\pi^-$ is often touted as a way to measure $\sin 2\alpha$. In the absence of penguin diagrams, this is certainly true. However, penguin diagrams are expected to make a significant contribution to this decay mode, greatly complicating the extraction of CKM information from the observed *CP* asymmetry.

Many studies have been done of how to obtain precision CKM information from the *CP* asymmetry, including measurement of the decay mode $B^0 \to \pi^0\pi^0$ and detailed analysis of the Dalitz plot in the similar $B^0 \to \rho\pi$ mode. These methods are complicated and difficult for any experiment and are not feasible for CDF due to the necessity of accurately and efficiency detecting π^0's.

We have investigated a very promising method suggested by Fleischer [21] that measures the CKM angle γ by relating the *CP* violation observables in the decays $B^0 \to \pi^+\pi^-$ and $B_s^0 \to K^+K^-$. The necessity of the B_s^0 mode makes this strategy unique and well suited to the Tevatron.

The decays $B^0 \to \pi^+\pi^-$ and $B_s^0 \to K^+K^-$ are related to each other by interchanging all down and strange quarks, that is, through the so-called "U-spin" subgroup of the SU(3) flavor symmetry of strong interactions. For the decay $B^0 \to \pi^+\pi^-$, the tree diagram is expected to be dominant with the penguin diagram being subdominant (but significant). For the decay $B_s^0 \to K^+K^-$, the opposite is expected, that is, the penguin diagram is expected to dominate. The strategy in reference [21] uses the U-spin symmetry to relate the ratio of hadronic matrix elements for penguins and trees, and thus uses $B_s^0 \to K^+K^-$ to correct for the penguin pollution in $B^0 \to \pi^+\pi^-$.

This strategy does not rely on "plausible" dynamical or model-dependent assumptions, nor on final-state interaction effects, as do many other methods of extracting γ. The theoretical accuracy is only limited by U-spin-breaking effects. We have evaluated the likely size of these effects and find them to be small compared to the expected experimental error on γ in Run II.

The key to measuring the *CP* asymmetries in $B^0 \to \pi^+\pi^-$ and $B_s^0 \to K^+K^-$ is to trigger on these decays in hadronic collisions. We will do this with the two displaced tracks trigger, which is a significant fraction of the Level 1 bandwidth in Run IIa. To maintain the viability of this trigger in Run IIb, we will add the ability to obtain three dimensional tracking information and make an invariant mass selection in Level 1.

Observation of these modes is further complicated by similar branching ratios for the modes $B^0, B_s^0 \to K\pi$ and the lack of good particle identification in CDF. The CLEO, Babar, and Belle experiments have measured $Br(B^0 \to K^+\pi^-) = (17.3 \pm 1.5) \times 10^{-6}$ and $Br(B^0 \to \pi^+\pi^-) = (4.4 \pm 0.9) \times 10^{-6}$ (these are weighted averages of the results in [22]). The corresponding B_s^0 decays have not been observed, but we can make an educated guess based on SU(3) symmetry, giving

$$Br(B_s^0 \to K^+K^-) = (F_K/F_\pi)^2 \times Br(B^0 \to K^+\pi^-) \quad (2.9)$$

$$Br(B_s^0 \to \pi^+K^-) = (F_K/F_\pi)^2 \times Br(B^0 \to \pi^+\pi^-) \quad (2.10)$$

where $(F_K/F_\pi)^2 = 1.3$ accounts for SU(3) breaking. Taking into account the production ratio of $f_s/f_d \sim 0.4$, we expect the following relative yields:

$$(B^0 \to K\pi) : (B^0 \to \pi\pi) : (B_s^0 \to KK) : (B_s^0 \to \pi K) \sim 4 : 1 : 2 \quad (2.11)$$

Based on the measured branching ratios, our observed Run I B cross sections, and Monte Carlo studies, we expect 20,000 $B^0 \to K^\pm\pi^\mp$; 5,000 $B^0 \to \pi^+\pi^-$; 10,000 $B_s^0 \to K^+K^-$; and 2,500 $B_s^0 \to K^\mp\pi^\pm$ events in Run IIa, with an expected increase of a factor of 7.5 in Run IIb. Special runs in Run I were used to estimate the signal to background to be roughly

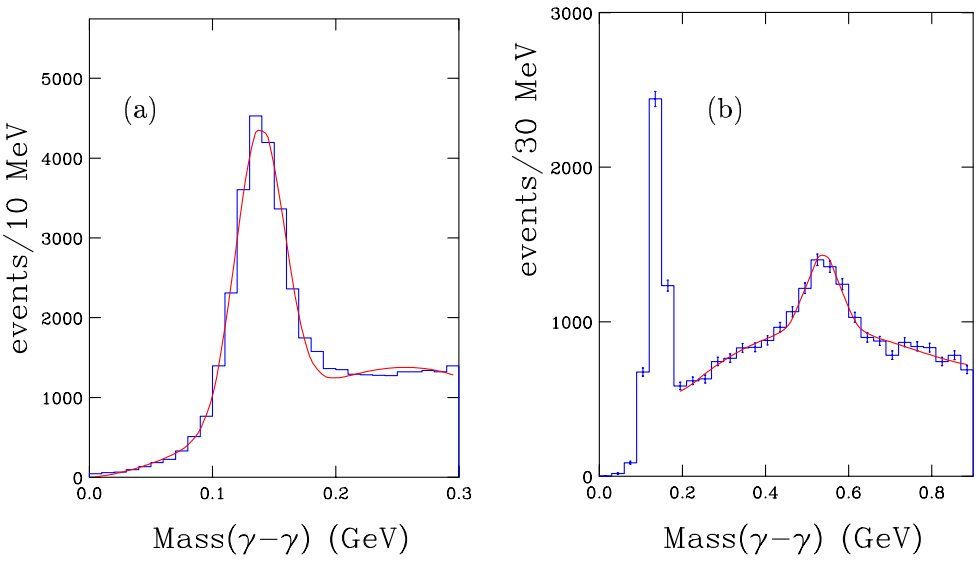

Figure 2.66: Invariant diphoton mass distribution showing (a) $\pi^0 \to \gamma\gamma$ and (b) $\eta \to \gamma\gamma$ signals in CDF Run I data.

0.4, although we expect the 3-dimensional vertexing capability in Run II to improve this. Figure 2.67 shows the expected invariant mass peak for the number of signal events above with 56,250 background events. The signals overlap, but detailed studies have shown it is possible to extract the *CP* asymmetries by exploiting the excellent mass resolution of CDF, dE/dx information from the COT, and the greatly different oscillation frequencies of the B^0 and B_s^0 mesons.

Detailed studies of the expected error on the *CP* asymmetries show that γ can be measured to $\sim \pm 10°$ with a four-fold ambiguity in Run IIa, assuming that $\sin 2\beta$ is precisely known from $B^0 \to J/\psi K_s$. By allowing 20% SU(3) symmetry breaking, we estimate the theoretical uncertainty to be $\sim \pm 3°$. With the increased luminosity of Run 2b, the statistical uncertainty should be $\sim \pm 3°$, making this a very promising method for measurement of γ.

2.7.5.5 Measuring γ With $B_s^0 \to D_s^{\mp} K^{\pm}$ Decays

CP violation occurs in $B_s^0 \to D_s K$ decays via interference between direct decays $B_s^0 \to D_s^{\mp} K^{\pm}$ and cases where the B_s^0 first mixes to a $\overline{B}_s^0$ with the subsequent decay $\overline{B}_s^0 \to D_s^{\mp} K^{\pm}$. Since B_s^0 mixing is expected to have very small *CP* violating phase, the relative phase of these decays is $e^{i\gamma}$, and penguin contributions are expected to be small, these decays potentially give a theoretically clean measurement of γ. Since the final states are not *CP* eigenstates, there is a strong phase δ which cannot be reliably calculated with present theoretical techniques.

The time dependent decay rate for these four processes are

$$\begin{aligned}
\Gamma(B_s^0 \to D_s^- K^+) &= \frac{|A|^2 e^{-\Gamma_s t}}{2}\{(1+|\lambda|^2)\cosh(\Delta\Gamma_s t/2) + (1 \\
&\quad -2|\lambda|\cos(\delta+\gamma)\sinh(\Delta\Gamma_s t/2) - 2|\lambda|\sin \\
\Gamma(B_s^0 \to D_s^+ K^-) &= \frac{|A|^2 e^{-\Gamma_s t}}{2}\{(1+|\lambda|^2)\cosh(\Delta\Gamma_s t/2) - (1 \\
&\quad -2|\lambda|\cos(\delta-\gamma)\sinh(\Delta\Gamma_s t/2) + 2|\lambda|\sin \\
\Gamma(\overline{B}_s^0 \to D_s^- K^+) &= \frac{|A|^2 e^{-\Gamma_s t}}{2}\{(1+|\lambda|^2)\cosh(\Delta\Gamma_s t/2) - (1 \\
&\quad -2|\lambda|\cos(\delta+\gamma)\sinh(\Delta\Gamma_s t/2) + 2|\lambda|\sin \\
\Gamma(\overline{B}_s^0 \to D_s^- K^+) &= \frac{|A|^2 e^{-\Gamma_s t}}{2}\{(1+|\lambda|^2)\cosh(\Delta\Gamma_s t/2) + (1 \\
&\quad -2|\lambda|\cos(\delta-\gamma)\sinh(\Delta\Gamma_s t/2) - 2|\lambda|\sin
\end{aligned}$$

where $|A|$ is the magnitude of the $B_s^0 \to D_s^- K^+$ amplitude and $|\lambda|$ is the magnitude of the ratio of this amplitude to the one for $B_s^0 \to D_s^+ K^-$.

By fitting the time dependent decay rates for these four modes, the parameters $|A|$, $|\lambda|$, and $\delta \pm \gamma$ can be extracted. Since the rates depend on $\sin(\delta \pm \gamma)$ and $\cos(\delta \pm \gamma)$, there is a two fold ambiguity, namely,

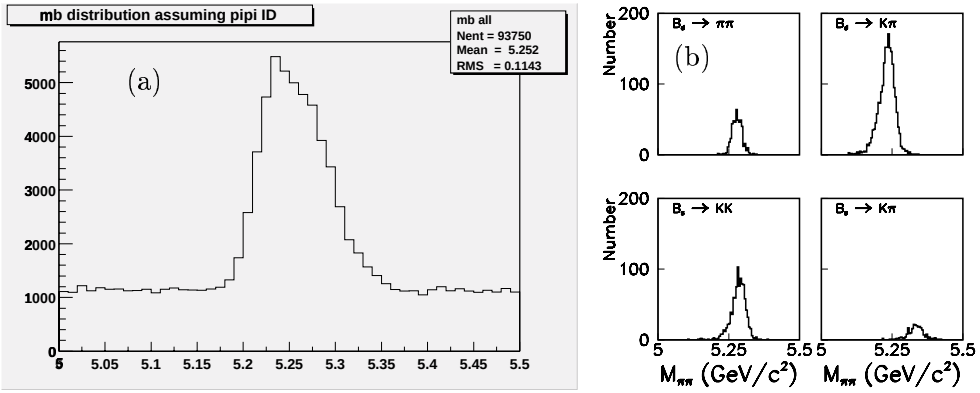

Figure 2.67: Two-track invariant mass assuming pion hypothesis for $B \to \pi\pi, K\pi, KK$, and πK states (a) added together and (b) shown separately.

(δ, γ) and $(\delta + \pi, \gamma + \pi)$ are equivalent solutions. If $\Delta\Gamma_s/\Gamma_s$ is sufficiently small that the sinh terms cannot be resolved, then there an 8-fold ambiguity in the solutions.

The branching ratios for the decays $B_s^0 \to D_s^- K^+$ and $B_s^0 \to D_s^+ K^-$ are expected to be comparable, namely, 2.4×10^{-4} and 1.4×10^{-4}, respectively. In Run IIa, these events would satisfy the displaced track trigger. Monte Carlo studies indicate that CDF expects to reconstruct about 850 $B_s \to D_s^- K^+$ events in the Run IIa data. Studies of Run I data indicate that the signal to background ratio should be between 0.5 and 2, not including improvements that may be made with dE/dx information and 3-dimensional vertexing. With these conditions, we expect to measure $\sin(\delta \pm \gamma)$ to around 0.4 to 0.7 in Run IIa.

In Run IIb, if we can maintain the trigger rates, we would expect a factor of three improvement, which begins to place significant limits on γ, assuming that the sinh term is measurable or that δ is reliably determined theoretically (otherwise, the multiple ambiguities still allow most values of γ). However, as discussed above, the rate for the displaced track trigger is problematical in Run IIb, and since these are multibody decays, they would not pass a two-body invariant mass cut in Level 1. Another option is trigger scenario C described above, which can operate at the high instantaneous luminosities of Run IIb, but which has half the yield for signal events.

2.7.5.6 Measuring γ With $B^- \to D^0 K^-$ Decays

In a similar manner, the angle γ can be determined from the decays $B^- \to D^0 K^-$ and $B^- \to \overline{D}^0 K^-$ where the D^0 and $\overline{D}^0$ decay to both $K^\pm \pi^\mp$. Note that these modes are self-tagging and no time dependent measurement is necessary. However, the significant difference in the branching ratios limit CP violating effects to $\mathcal{O}(10\%)$.

Table 2.16 shows the branching ratios for the relevant modes. The decay $B^- \to K^- \overline{D}^0$ is particularly problematic due to the small expected branching ratio. All these decays have significant physics and combinatoric backgrounds that must be reduced to acceptable to make this method feasible. Studies show that physics backgrounds from similar modes and particle misassignments can be reduced to about the same level as the signals by using invariant mass selections and dE/dx information. These modes also have the problem that they are multi-body and hence are problematic for the displaced track trigger in Run IIb.

If the combinatoric backgrounds can be controlled and the decay $B^- \to \overline{D}^0 K^-$ measured to about 20%, then γ could be determined to about 15°.

2.7.5.7 Direct CP Violation in $\Lambda_b \to pK, p\pi$

It should also be possible to observe direct CP violation in B decays, the analog in the B system to measuring ϵ'/ϵ in the neutral kaon system. It is most straight-forward to do this in decays where the de-

$\mathrm{BR}(B^+ \to K^+\overline{D}^0) = 2.6 \pm 0.08 \times 10^{-4}$	CLEO
$\mathrm{BR}(B^+ \to K^+D^0) \approx 2 \times 10^{-6}$	Estim. [23]
$\mathrm{BR}(\overline{D}^0 \to K^-\pi^+) = 1.3 \pm 0.3 \times 10^{-4}$	CLEO
$\mathrm{BR}(\overline{D}^0 \to K^+\pi^-) = 3.8 \pm 0.1 \times 10^{-2}$	PDG

Table 2.16: Estimated branching ratios of decays involved in the analysis of $B^- \to D^0K^- \to [K\pi]K^-$ at CDF.

cay products tag the flavor of the original B hadron (called self-tagging modes). Any B^+ or Λ_b mode has this feature, as do some B^0 and B_s^0 modes.

As an example, we discuss the decays $\Lambda_b \to p\pi^-$ and $\Lambda_b \to pK^-$. The asymmetry in this case is defined to be

$$A = \frac{\Lambda_b - \overline{\Lambda}_b}{\Lambda_b + \overline{\Lambda}_b}, \tag{2.12}$$

where Λ_b and $\overline{\Lambda}_b$ refer to the number of each type observed. In the Standard Model, the asymmetry for $\Lambda_b \to pK$ is expected to be about 10%, whereas the asymmetry for $\Lambda_b \to p\pi$ is predicted to be in the 20% to 30% range.

The branching ratios for these modes are not known, but are estimated to be similar to $B^0 \to \pi\pi$. Since these Λ_b decay modes will satisfy the two displaced track trigger (assuming the mass windows are chosen appropriately), the number of expected events in each mode can be scaled from the number of expected $B^0 \to \pi\pi$ and the relative production rates, giving 10,000 events in 15 fb^{-1}. An advantage to this measurement is that tagging is not necessary, thus all the events are fully available for the asymmetry measurement. The background for these modes should be no worse than for $B^0 \to \pi\pi$, and use of TOF and dE/dx may substantially reduce them. We assume a signal to background of 1 to 2.

There is also a possibility of accepting a combination that interchanges the p and the K or π, which is essentially a mistag. Using the TOF system, this can be reduced to about 10% at a 20% loss of signal.

The formula for the uncertainty on the asymmetry in the presence of background and mistagging for small asymmetries is

$$\sigma_A = \frac{1}{D}\sqrt{\frac{S+B}{S^2}}, \tag{2.13}$$

where A is the asymmetry, S is the number of signal events, B is the number of background events, $D = 1-2f$ is the dilution factor due to mistags, and f is the mistag rate. Thus, we expect an error on the asymmetry of about 2%, significantly smaller than the Standard Model predicted asymmetries. Note there will also be a systematic error due to the mistagging, but we should be able to keep this at the level of 1% or smaller.

2.7.6 Mixing and Lifetime Differences

One of the primary goals of CDF in Run IIa is to observe B_s^0 mixing. The ratio of oscillation frequency Δm_s to the oscillation frequency Δm_d determines the ratio $|V_{td}/V_{ts}|$ up to theoretical uncertainties on the order of 5-10%.

With the addition of Layer 00 for excellent vertex resolution and the displaced track trigger to give a large sample of exclusive decays (such as $B_s^0 \to D_s\pi$), CDF expects to have a reach in Δm_s which is far beyond the Standard Model expectation. Furthermore, once a statistically significant signal is observed in B_s^0 oscillations, the value of Δm_s has a very small statistical uncertainty. Thus, we expect that B_s^0 mixing will be observed in Run IIa, and its usefulness for determining $|V_{td}/V_{ts}|$ and constraining the unitarity triangle will be limited by theoretical uncertainties.

CDF will continue to pursue measurements of B^0 and B_s^0 mixing in Run IIb since precise knowledge of Δm_d and Δm_s is necessary for extraction of other physics signals, such as, time dependent CP asymmetries in B^0 and B_s^0 decays. However, we do not expect further improvements in these measurements to directly impact our understanding of CKM physics.

2.7.6.1 $\Delta\Gamma_s/\Gamma_s$

The calculation of Δm_s depends upon the evaluation of the real part of the mass matrix element. The imaginary part of the same matrix describes the decay widths of the two mass eigenstates B_s^H and B_s^L. Within the Standard Model it is possible to calculate the ratio $\Delta\Gamma_s/\Delta m_s$ [24]:

$$\Delta\Gamma_s/\Delta m_s = -\frac{3}{2}\pi\frac{m_b^2}{m_t^2}\frac{\eta_{QCD}^{\Delta\Gamma_s}}{\eta_{QCD}^{\Delta m_s}} \tag{2.14}$$

where the ratio of the QCD correction factors (η) in the numerator and denominator is expected to be of order unity [25]. This ratio does not depend on CKM parameters. Thus, a measurement of $\Delta\Gamma_s$ determines Δm_s up to QCD uncertainties. Moreover, the larger

Δm_s becomes the larger $\Delta\Gamma_s$ is. Thus, as it becomes more difficult to measure Δm_s, $\Delta\Gamma_s$ becomes more accessible. Using the above expression, Browder *et al.* [25] show that if $x_s = 15$, a 7% difference in lifetime is expected.[2] They estimate that the uncertainties in calculating $\Delta\Gamma_s/\Delta m_s$ contribute an uncertainty of $\sim 30\%$ on $|V_{td}/V_{ts}|^2$ (that is, a 15% uncertainty on $|V_{td}/V_{ts}|$). This contribution to the theoretical uncertainty should be added in quadrature to the 10% uncertainty discussed in the previous section, for a total uncertainty of $\approx 20\%$.

We do not expect $\Delta\Gamma_s/\Gamma_s$ to be measured sufficiently well in Run IIa that its usefulness is dominated by theoretical uncertainties. Thus, we will continue to pursue this measurement with the higher statistics available from Run IIb.

Several techniques can be used to determine $\Delta\Gamma_s$ [26]. First, the proper time distribution of a flavor-specific B_s^0 mode (*e.g.* $B_s^0 \to D_s \ell\nu$ or $B_s^0 \to D_s^- \pi^+$) can be fit to the sum of two exponentials, although for the small lifetime differences expected, this method is not efficient and not competitive with the ones below. Second, the average lifetime of such a flavor specific mode can be compared to the lifetime of a mode that is dominated by a single *CP* state (such as $B_s^0 \to D_s \overline{D}_s$) [27]. Finally, a decay such as $B_s^0 \to J/\psi\,\phi$ can be decomposed into its two *CP* components (via a transversity analysis [28]) and fit for a separate lifetime for each component. It is noted that CDF has measured the helicity structure of the decays $B \to J/\psi K^*$ and $B_s^0 \to J/\psi\phi$ using Run Ia data [8]. The results obtained for the parity-even fractions are $0.87^{+0.12}_{-0.09}$ for $B \to J/\psi K^*$ and 0.77 ± 0.19 for $B_s \to J/\psi\,\phi$.

The statistical uncertainty on the B_s^0 lifetime from semileptonic B decays in Run II will be below 1%. The Run II expectation is for $\approx 60,000$ $B_s^0 \to J/\psi\,\phi$ events in 15 fb^{-1}. The $B_s^0 \to J/\psi\phi$ helicity structure should then be known to about 1% [3]. Using the current CDF number for the $B_s^0 \to J/\psi\,\phi$ helicity structure, with 15 fb^{-1}, $\Delta\Gamma_s/\Gamma_s$ could be determined to 0.01. Including current theoretical uncertainties of 20%, this determination of $\Delta\Gamma_s$ would either measure $|V_{td}/V_{ts}|$ or set an *upper* bound on $x_s = \Delta m_s/\Gamma_s \leq 15$. Thus, using the direct x_s measurement and $\Delta\Gamma_s/\Gamma_s$, CDF II should be able to measure $|V_{td}/V_{ts}|$ over the full range permitted by the Standard Model in Run II.

It is important to note that the discussion of B_s^0 mixing (and *CP* violation) has been in the context of the three generation Standard Model. New physics associated with large mass scales can also reveal itself through a study of the mass and width differences for the neutral B mesons [29].

2.7.6.2 $\Delta\Gamma_d/\Gamma_d$

The lifetime difference for the B^0 eigenstates is expected to be very small in the Standard Model, around 0.3%. This is smaller than probably can be measured, even in Run IIb. However, the lifetime difference is sensitive to new physics and may be as large as a few per cent in some extensions to the Standard Model, which should be measurable.

The lifetime difference $\Delta\Gamma_d/\Gamma_d$ can be measured by comparing the lifetime measured in a high statistics *CP* eigenstate mode, such as $B^0 \to J/\psi K_s^0$, to the lifetime measured in a flavor specific mode, such as semileptonic decays or $B^0 \to J/\psi K^{*0}$,$K^{*0} \to K^+\pi^-$. Note that flavor tagging is not needed here and the full statistics of the samples are available.

For the ~150,000 $B^0 \to J/\psi K_s$ decays expected in Run IIb, the statistical error on the lifetime is $\sim 0.3\%$, comparable to the lifetime difference in the Standard Model. At this level, effects of backgrounds and other systematic effects are probably important, but significant deviations from the Standard Model prediction should be observable.

2.7.7 B_c^+ Decays

In Run I, CDF discovered the B_c^+ meson via its semileptonic decay $B_c^+ \to J/\psi\ell\nu X$ [10]. In Run II, we expect to observe this meson in several exclusive decay modes, making precise determination of its mass and lifetime possible.

One of the cleanest exclusive modes is $B_c^+ \to J/\psi\pi^+$. We estimate the number of expected events by scaling from the observed number of $B_c^+ \to J/\psi\ell\nu X$ events and theoretical predictions of the relative branching ratios [30], which range from 0.06 to 0.32. This gives us an expectation of 9 events in Run I on an observed background of roughly 6 events.

Extrapolating to Run IIb, including the detector and trigger improvements for Run II, we expect to ob-

[2] This large $\Delta\Gamma_s$ is possible because there are common decay modes with large branching fractions available to the B_s^0 and $\overline{B}_s^0$ (*e.g.* $D_s^{(*)+} D_s^{(*)-}$).

[3] The systematic uncertainties in the polarization measurements are dominated by the estimate of the size and helicity of the background under the B mass peak. These systematic uncertainties should scale with the square root of the number of events in the sample.

serve about 3000 $B_c^+ \to J/\psi\pi^+$ events. These events plus those from other exclusive decays will allow us to make very precise measurements of the B_c^+ mass and lifetime.

We also note that the decay $B_c^+ \to J/\psi\pi^+$ which may exhibit a *direct CP* violating effect at the few percent level [31]. The mode is self–tagging and no time dependence is required. Any non–vanishing effect would immediately exclude the superweak model of *CP* violation. In Run IIb, for 3000 events, we expect about a 2% error on the asymmetry.

The relatively short lifetime observed for the B_c^+ (albeit with large errors) indicates the it decays primarily by decay of the charm quark, that is, via the decay $B_c^+ \to B_s^0\pi^+$. Based on the approximately 150,000 fully reconstructed B_s^0 decays we expect in Run IIb, we should observe a few hundred $B_c^+ \to B_s^0\pi^+$ decays.

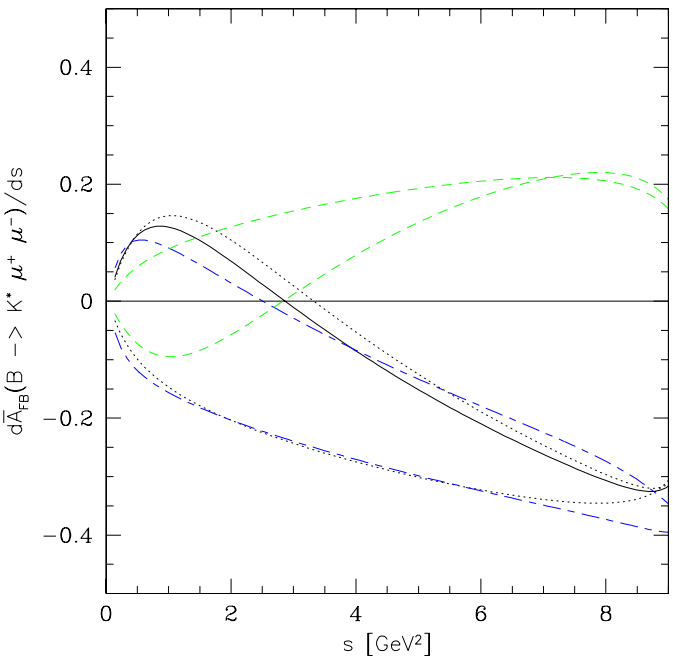

Figure 2.68: The forward-backward asymmetry in $B^0 \to K^{*0}\mu\mu$ decay as a function of $s = M_{\mu\mu}^2$ predicted by the Standard Model (solid line), the SUGRA (dotted), and MIA-SUSY (long-short dashed line) [32].

2.7.8 Rare B decays

Rare B decays provide a stringent test of the Standard Model for possible new physics effects, such as an anomalous magnetic moment of the W or the presence of a charged Higgs. Experimentally, rare decays such as $B^0 \to K^{*0}\mu\mu$, $B^0 \to \mu\mu$, and $B_s^0 \to \mu\mu$ are accessible via the dimuon trigger.

The straight dimuon trigger for muons outside the narrow J/ψ mass window will become problematical for the high luminosities of Run IIb. In Run IIa, we have implemented a dimuon trigger that requires an additional displaced track. It is expected that this trigger will be sufficient to search for rare B decays with dimuons in Run IIb.

2.7.8.1 $B^0 \to K^{*0}\mu\mu$

The decay $B^0 \to K^{*0}\mu\mu$ is expected in the Standard Model to have a branching ratio of approximately 1.5×10^{-6}. For this branching ratio, we expect to observe 36±7 events in Run IIa and 270±50 events in Run IIb with the dimuon plus displaced track trigger.

The forward-backward asymmetry A_{FB} of the muons relative to the B direction in the dimuon frame is expected to be extremely sensitive to new physics. In the Standard Model, A_{FB} is expected to cross zero as a function of the dimuon mass $M_{\mu\mu}$ at a value around 2 GeV/c^2. New physics can change, or even eliminate, where this zero crossing occurs. Figure 2.68 shows the expected forward-backward asymmetry as a function of $M_{\mu\mu}$ for the Standard Model and several possible extensions to the standard model.

Figure 2.69 shows the expected A_{FB} distribution with 50 and 400 $B^0 \to K^{*0}\mu\mu$ events after all trigger and offline requirements. The solid line in the figure corresponds to the Monte Carlo generated distribution. It is clear that the statistics in Run IIa will be marginal for extracting information on A_{FB}. The situation is still challenging in Run IIb but hopeful. We are exploring methods to best extract the zero crossing point of A_{FB}, including in the presence of backgrounds.

The statistics of Run IIb are definitely needed for this measurement. The events come from the dimuon plus displaced track trigger, which should not need to be prescaled in Run IIb.

2.7.8.2 $B \to \mu\mu$

The dimuon plus displaced track trigger is also useful to search for the two-body decays $B^0, B_s^0 \to \mu\mu$, predicted to have branching ratios of 1.5×10^{-9} and 3.5×10^{-8}, respectively. Since these branching ratios are at the limits of CDF's reach, even in Run IIb, we

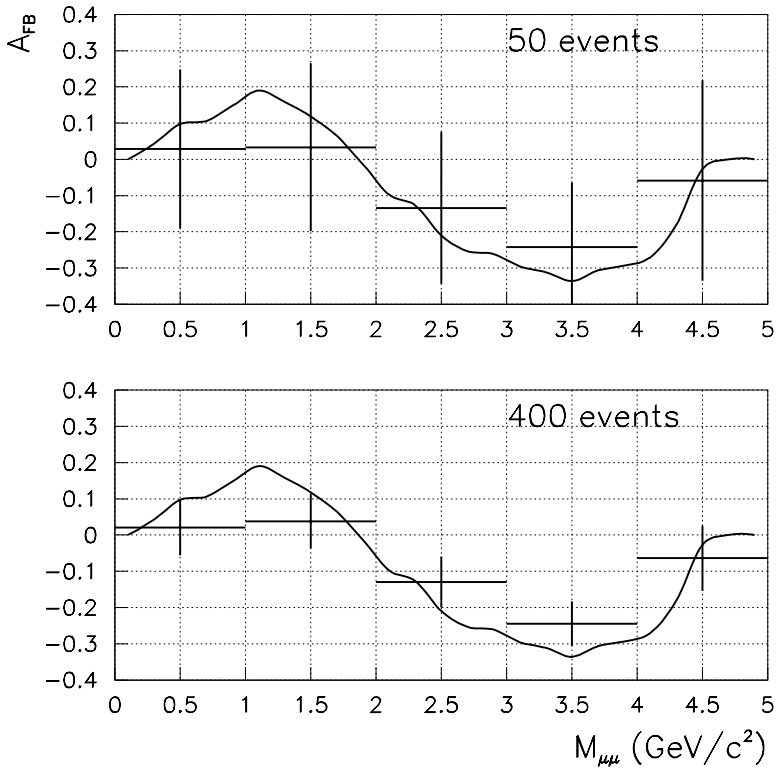

Figure 2.69: A_{FB} with 50 and 400 events of the $B^0 \to K^*\mu\mu$ signal and $S/B = 1$.

quote "single-event sensitivities", that is, the branching ratio for which we would expect one observed event in 15 fb^{-1}.

CDF searched for these decays in Run I [13] with single-event sensitivities of

$$S(B^0 \to \mu\mu) = (2.0 \pm 0.5) \times 10^{-7} \quad (2.15)$$
$$S(B_s^0 \to \mu\mu) = (6.0 \pm 1.6) \times 10^{-7}. \quad (2.16)$$

The Run IIb expectations extrapolated from these, including the difference in trigger, muon coverage, and cross section, are

$$S(B^0 \to \mu\mu) = 2.1 \times 10^{-9} \frac{15\text{fb}^{-1}}{\int \mathcal{L}(\text{fb}^{-1})} \quad (2.17)$$
$$S(B_s^0 \to \mu\mu) = 3.5 \times 10^{-8} \frac{15\text{fb}^{-1}}{\int \mathcal{L}(\text{fb}^{-1})}. \quad (2.18)$$

Thus, for the expected Standard Model branching fractions, we would expect to not see $B^0 \to \mu\mu$ and to see a few $B_s^0 \to \mu\mu$ events.

Note that it is possible for new physics (such as a charged Higgs) to substantially increase these branching fractions, to which we would be sensitive. Also note, that we have not yet done an extensive study of the backgrounds expected at these levels, which, of course, is crucial for understanding whether we could actually see a signal above the background.

2.7.9 Radiative B Decays

In the absence of long distance effects, radiative B decays provide an alternative approach for measuring $|V_{td}/V_{ts}|$. Radiative decays are also interesting because they proceed solely through penguin diagrams. It is likely that the B factory experiments will measure B^- and B^0 radiative decays better than is possible at CDF. Still, CDF will measure radiative decays, including B_s^0 and Λ_b radiative decays, which are not accessible to the B factories.

CDF will use two methods to search for radiative penguin decays. The first identifies photons as clusters in the Central EM calorimeter. For Run II, a trigger requiring a 5 GeV EM cluster (the photon) and two tracks above 1.5 GeV/c is being implemented. From this trigger, we expect to observe ~ 2700 $B^0 \to K^*\gamma$ events in 2 fb^{-1} for a branching ratio of 4.5×10^{-5}. The mass resolution of the reconstructed B is dominated by the resolution on the

photon energy and is $\sim$ 140 MeV. We have studied our ability to reject combinatorial background using Run I photon data and have studied with Monte Carlo the discrimination against $B \to K^*\pi^0$ and $\rho\pi^0$ and higher multiplicity penguin decays [34]. These backgrounds are manageable. However, the offline cuts to remove background are expected to reduce the signal by about a factor of 2. The mass resolution is not adequate to separate $\gamma\rho$ from γK^* on an event-by-event basis; however, a statistical separation is possible. In addition, the COT dE/dx system should provide 1σ K-π separation in the momentum range of interest.

The second method looks for photon conversions where the electron or positron satisfies the 4 GeV electron with displaced track trigger. The probability for a photon to convert in the material around the beam pipe in Run I was $\sim$ 5%, which is expected to increase to $\sim$ 10% in Run II due to additional material in SVX II. The main advantage of the conversion method is that the B mass is calculated solely from charged tracks, giving a resolution comparable to B signals observed in Run I, that is, 20 to 30 MeV/c^2. The backgrounds are also less for the conversion sample. The improved resolution gives cleaner signals and allows separation of $B^0 \to \rho\gamma$, $B^0 \to K^*\gamma$, and $B_s^0 \to K^*\gamma$ signals. These advantages will probably make the conversion method the optimal one for Run II.

The numbers of radiative penguin decays expected in the conversion sample in Run 2 are

$$N(B^0 \to K^*\gamma) = 170 \times \frac{\int \mathcal{L}(\mathrm{fb}^{-1})}{2\mathrm{fb}^{-1}} \times \frac{Br(B_d \to K^*\gamma)}{4.5 \times 10^{-5}} \quad (2.19)$$

$$N(B_s^0 \to \phi\gamma) = 63 \times \frac{\int \mathcal{L}(\mathrm{fb}^{-1})}{2\mathrm{fb}^{-1}} \times \frac{Br(B_d \to K^*\gamma)}{4.5 \times 10^{-5}} \quad (2.20)$$

$$N(B_s^0 \to K^*\gamma) = 2.2 \times \frac{\int \mathcal{L}(\mathrm{fb}^{-1})}{2\mathrm{fb}^{-1}} \times \frac{Br(B_d \to K^*\gamma)}{4.5 \times 10^{-5}} \quad (2.21)$$

$$N(\Lambda_b \to \Lambda\gamma) = 5 \times \frac{\int \mathcal{L}(\mathrm{fb}^{-1})}{2\mathrm{fb}^{-1}} \times \frac{Br(B_d \to K^*\gamma)}{4.5 \times 10^{-5}} \quad (2.22)$$

Thus, the 15 fb^{-1} of Run IIb will be needed to observe the $B_s^0 \to K^*\gamma$ and $\Lambda_b \to \Lambda\gamma$ modes.

2.7.10 Semileptonic Decays

In Run II, CDF will observe large numbers of semileptonic decays of all species of B hadrons. Here, we concentrate on $\Lambda_b \to \Lambda_c\ell\nu$ decays, which are not produced in e^+e^- B factories, as being illustrative. Semileptonic decays of B hadrons are acquired via the inclusive electron and muon triggers. For B physics, the rates for these triggers can be kept under control by also requiring a displaced track.

Measuring the differential decay rate $(1/\Gamma)\, d\Gamma/dQ^2$, where Q^2 is the momentum transfer, is a stringent test of Heavy Quark Effective Theory (HQET). These tests require large data samples and so are ideally suited to Run II. In the Run I Λ_b lifetime analysis, 197$\pm$25 $\Lambda_b \to \Lambda_c\ell\nu$, $\Lambda_c \to pK\pi$ events were partially reconstructed [6]. Extrapolating to Run IIb, including the improvements in the detector and trigger, gives an expected yield of 150,000 events in 15 fb^{-1}.

Tests of HQET in Λ_b semileptonic decays could be compromised by contamination from decays of the Λ_b to higher order charmed baryons. Monte Carlo studies show that rejection of events with extra tracks having a small impact parameter with respect to the Λ_b vertex controls these backgrounds at acceptable levels.

2.7.11 $\psi(2S)$ Polarization

In Run I, CDF measured the direct production of both J/ψ and $\psi(2S)$ mesons, giving cross-sections approximately 50 times greater than those predicted by QCD using the color-singlet model. This anomalous production can be explained in nonrelativistic QCD by the inclusion of color-octet $c\overline{c}$ states in the hadronization process. A consequence of this production mechanism is that the transverse polarization of the J/ψ and $\psi(2S)$ mesons approaches 100% for transverse momenta $p_T \gg m_c$, where m_c is the charm quark mass. Measurements in Run I by CDF of the J/ψ and $\psi(2S)$ polarizations [35] did not support the color octet models, but statistics were limited at large transverse momenta, where the theory is most reliable.

In Run IIa, the uncertainties on the polarization of J/ψ's will be $\pm$0.2 at a transverse momentum of 30 GeV/c, providing a stringent test of the color octet models. However, direct J/ψ's have the problem that some of them come from decays of prompt $\psi(2S)$'s and χ states, adding some uncertainty to the interpretation of the measurement. Direct $\psi(2S)$'s do not have this problem, but to measure their polarization out to comparable transverse momenta will require the statistics of Run IIb.

2.7.12 Concluding remarks

From the previous discussion it should be clear that in Run IIb CDF plans to fully exploit the copious production of all species of b hadrons at the Tevatron. We believe we will have a complete and competitive program, with unique strengths, for example, in rare decays and B_s^0 physics.

With the experience gained so far in the analyses of Run I data and the planned capabilities of the CDF II detector, we are able to confidently project our expectations for Run IIa and Run IIb which include:

- Observation of *CP* violation in $B^0 \to J/\psi K_S^0$ and measurement of $\sin(2\beta)$ to better than ± 0.02.
- Measurement of the *CP* asymmetries in $B_s^0 \to J/\psi\,\phi, J/\psi\eta^{(\prime)}$, which measure the phase of V_{ts} in the Standard Model and are sensitive to new *CP* violating physics.
- Observation of *CP* violation in $B^0 \to \pi^+\pi^-$, $B_s^0 \to K^+K^-$ and measurement of the unitarity triangle angle γ to better than $\pm 3^\circ$.
- Observation of B_s^0 mixing and precise determination of Δm_s.
- Measurement of $\Delta\Gamma_s/\Gamma_s$ to 0.01.
- Observation of exclusive decay modes of the B_c^+ meson, allowing precise determinations of its mass and lifetime.
- Observation of radiative penguin decays.
- Observation of the rare decays $B^0 \to \mu\mu K^{*0}$ and $B^\pm \to \mu\mu K^\pm$.

With these and other measurements that we will pursue with b hadrons in Run IIa and Run IIb, we expect to greatly improve the understanding of weak-interaction quark mixing and *CP* violation in the Standard Model and be very sensitive to new physics in these areas.

Bibliography

[1] L. Wolfenstein, Phys. Rev. Lett. **51**, 1945 (1984).

[2] "Measurement of the Mass of the B_s^0 Meson." F. Abe *et al.*, Phys. Rev. **D53** 3496 (1996); "Observation of the Decay $B_s^0 \to J/\psi\,\phi$ in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV." F. Abe *et al.*, Phys. Rev. Lett. **71** 1685 (1993).

[3] "Observation of $\Lambda_b \to J/\psi\Lambda^0$ at the Fermilab Proton–Antiproton Collider." F. Abe *et al.*, Phys. Rev. **D55** 1142 (1997).

[4] "Measurement of the Average Lifetime of B Hadrons Produced in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV." F. Abe *et al.*, Phys. Rev. Lett. **71** 3421 (1993); "Measurement of the B^+ and B^0 Meson Lifetimes." F. Abe *et al.*, Phys. Rev. Lett. **72** 3456 (1994); "Measurement of the B^- and $\overline{B}^0$ Meson Lifetimes Using Semileptonic Decays." F. Abe *et al.*, Phys. Rev. Lett. **76** 4462 (1996); "Measurement of B Hadron Lifetimes Using J/ψ Final States at Cdf." F. Abe *et al.*, Phys. Rev. **D57** 5382 (1998); "Measurement of the B^- and $\overline{B}^0$ Meson Lifetimes Using Semileptonic Decays." F. Abe *et al.*, Phys. Rev. **D58** 092002 (1998).

[5] "Measurement of the B_s^0 Meson Lifetime." F. Abe *et al.*, Phys. Rev. Lett. **74** 4988 (1995); "Measurement of the Lifetime of the B_s^0 Meson Using the Exclusive Decay Mode $B_s^0 \to J/\psi\,\phi$." F. Abe *et al.*, Phys. Rev. Lett. **77** 1945 (1996); "Measurement of the B_s^0 Meson Lifetime Using Semileptonic Decays." F. Abe *et al.*, Phys. Rev. **D59** 032004 (1999).

[6] "Measurement of Λ_b^0 Lifetime Using $\Lambda_b^0 \to \Lambda_c^+\ell^-\bar{\nu}_\ell$." F. Abe *et al.*, Phys. Rev. Lett. **77** 1439 (1996).

[7] "Measurement of the *CP*-violation Parameter $\sin 2\beta$ in $B^0/\overline{B}^0 \to J/\psi K_s^0$ Decays." F. Abe *et al.*, Phys. Rev. Lett. **81** 5513 (1998); "A Measurement of $\sin 2\beta$ from $B \to J/\psi K_s^0$ with the CDF Detector." T. Affolder *et al.*, Phys. Rev. **D61** 072005 (2000).

[8] "Measurement of the Polarization in the Decays $B_d^0 \to J/\psi K^{*0}(892)$ and $B_s^0 \to J/\psi\phi$." F. Abe *et al.*, Phys. Rev. Lett. **75** 3068 (1995); "Measurement of the Polarization in the Decays $B_d^0 \to J/\psi K^{*0}(892)$ and $B_s^0 \to J/\psi\phi$." T. Affolder *et al.*, Phys. Rev. Lett. **85** 4668 (2000).

[9] *CP* Violation chapter of the Proceedings of the Fermilab Workshop on B Physics at the Tevatron: Run II and Beyond (known at the Yellow Book), to be published.

[10] "Observation of the B_c Meson in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV." F. Abe *et al.*, Phys. Rev. Lett. **81** 2432 (1998); "Observation of the B_c Meson in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV." F. Abe *et al.*, Phys. Rev. **D58** 112004 (1998); "Measurement of the Branching Fraction for $B^+ \to J/\psi\pi^+$ and Search for $B_c^+ \to J/\psi\pi^+$." F. Abe *et al.*, Phys. Rev. Lett. **77** 5176 (1996).

[11] "Measurement of $B^0\overline{B}^0$ Flavor Oscillation Frequency and Study of Same Side Flavor Tagging of B Mesons in $p\overline{p}$ Collisions." F. Abe *et al.*, Phys. Rev. **D59** 032001 (1999); "Measurement of the $B^0\overline{B}^0$ Oscillation Frequency Using Dimuon Data." F. Abe *et al.*, Phys. Rev. **D60** 051101 (1999); "Measurement of $B^0\overline{B}^0$ Flavor Oscillations Using Jet Charge and Lepton Flavor Taggin in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV." F. Abe *et al.*, Phys. Rev. **D60** 072003 (1999); "Measurement of the $B^0\overline{B}^0$ Oscillation Frequency Using $\ell^- D^{*+}$ Pairs and Lepton Flavor Tags." T. Affolder *et al.*, Phys. Rev. **D60** 112004 (1999).

[12] "Search for B_s^0 Oscillations Using the Semileptonic Decay $B_s^0 \to \phi\ell X\nu$." F. Abe *et al.*, Phys. Rev. Lett. **82** 3576 (1999).

[13] "Search for Flavor Changing Neutral Current in B Meson Decays in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$

TeV." F. Abe *et al.*, Phys. Rev. Lett. **76** 4675 (1996); "Search for the Decays $B^0 \to \mu^+\mu^-$ and $B_s^0 \to \mu^+\mu^-$ in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV." F. Abe *et al.*, Phys. Rev. **D57** R3811 (1998); "Search the Decays $B_s^0, B_d^0 \to e^{+-}\mu^{-+}$ and Pati-Salam Leptoquarks." F. Abe *et al.*, Phys. Rev. Lett. **81** 5742 (1998); "Search for Flavor-Changing Neutral Current Decays $B^+ \to \mu^+\mu^-K^+$ and $B^0 \to \mu^+\mu^-K^{*0}$." T. Affolder *et al.*, Phys. Rev. Lett. **83** 3378 (1999);

[14] "A Measurement of the B Meson and b Quark Cross Sections at $\sqrt{s}$ =1.8 TeV Using the Exclusive Decay $B^\pm \to J/\psi K^\pm$." F. Abe *et al.*, Phys. Rev. Lett. **68** 3403 (1992); "Measurement of the Bottom Quark Production Cross Section Using Semileptonic Decay Electrons in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV". F. Abe *et al.*, Phys. Rev. Lett. **71** 500 (1993); "Measurement of Bottom Quark Production in 1.8-TeV $p\overline{p}$ Collisions Using Semileptonic Decay Muons." F. Abe *et al.*, Phys. Rev. Lett. **71** 2396 (1993); "Measurement of the B Meson and b Quark Cross Sections at $\sqrt{s}$ =1.8-TeV using the Exclusive Decay $B_d^0 \to J/\psi K^{*0}(892)$." F. Abe *et al.*, Phys. Rev. **D50** 4252 (1994). "Measurement of the B Meson Differential Cross Section, $\frac{d\sigma}{dP_t}$, in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV." F. Abe *et al.*, Phys. Rev. Lett. **75** 1451 (1995); "Measurement of $b\bar{b}$ Rapidity Correlations in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV." F. Abe *et al.*, Phys. Rev. **D61** 032001 (2000).

[15] "Measurement of Correlated $\mu - \bar{b}$ Jet Cross Sections in $p\overline{p}$ Collisions at $\sqrt{s}$ =1.8 TeV." F. Abe *et al.*, Phys. Rev. **D53** 1051 (1996). "Measurements of $b\bar{b}$ Production Correlations, $B\bar{B}$ Mixing and a Limit on ϵ_B." F. Abe *et al.*, Phys. Rev. **D55** 2546 (1997).

[16] "Observation of *CP* Violation in the B^0 Meson System." BABAR collaboration, SLAC-PUB-8904, hep-ex/0107013, and submitted to Phys. Rev. Lett., July, 2001.

[17] "Observation of Large *CP* Violation in the Neutral B Meson System." Belle collaboration, Phys. Rev. Lett. **87** 091802 (2001).

[18] H. Quinn, B^0–$\bar{B}^0$ *Mixing and CP Violation in B Decay*, in Review of Particle Properties, Phys. Rev. **D50**, 1632 (1994) and references therein.

[19] "Proposal for Enhancement of the CDF II Detector: An Inner Silicon Layer and a Time of Flight Detector,", CDF II Collaboration, Fermilab-Proposal-909, October 1998; "Update to Proposal P-909: Physics Performance of the CDF II Detector with an Inner Silicon Layer and a Time of Flight Detector," Cdf II Collaboration, January 1999.

[20] The CDF Collaboration, *SVXII Simulation Study and Upgrade Proposal*, CDF Note 1922, (see in particular Table 13).

[21] R. Fleischer, Phys. Lett.**B459**.306 (1999).

[22] D. Cronin-Hennessy, *et al.* (CLEO), Phys. Rev. Lett **85**, 515 (2000); K. Abe, *et al.* (Belle), Phys. Rev. Lett **87**, 101801 (2001); B. Aubert, *et al.* (Babar), Phys. Rev. Lett **87**, 151802 (2001)

[23] D. Atwood, I. Dunietz, and A. Soni, Phys. Rev. Lett. **78**, 3257 (1997).

[24] J. Hagelin, Nucl. Phys. **B193**, 123 (1981); M.B. Voloshin *et. al* Sov. J. Nucl. Phys. **46**, 112 (1987).

[25] T.E. Browder and S. Pakvasa, UH 511-814-95. See also the recent discussion by M. Beneke, G. Buchalla and I. Dunietz, SLAC-PUB-7165, HEP-PH/9605259.

[26] I. Dunietz, Phys. Rev. **D51**, 2471 (1995).

[27] I. Bigi *et al.*, in "B Physics", 2nd edition, S. Stone editor.

[28] A.S. Dighe, I. Dunietz, H.J. Lipkin and J.L. Rosner, Phys. Lett. **B369**, 144 (1996).

[29] See Y. Grossman, WIS-96/13/Mar-PH, HEP-PH/9603244;
M. Gronau and D. London, Technion-PH-96-37, HEP-PH/9608430, and Y. Nir, WIS-96/31/Jul-PH, HEP-PH/9607415 for recent discussions.

[30] C. H. Chang and Y. Q. Chen, Phys. Rev. **D49**, 3399 (1994); S. S. Gershstein *et al.*, "Physics of B_c Mesons", Phys. Usp. **38**,1 (1995); S.

S. Gershstein *el al.*, "Theoretical Status of the B_c Meson", hep-ph/9803433, 24 March 1998; Rk K. Ellis, V. V. Kiselev, and A. K. Likhoded, "Theoretical Status of B_c Decays and Lifetimes", Yellow Book contribution (B Physics at the Tevatron: Run-2 and Beyond), December 1999; J. D. Bjorken, "Estimate of Decay Branching Ratios for Hadrons Containing Charm and Bottom Quarks", unpublished report (1986), http://www-theory.fnal.gov/people/ellis/Bphysics/bjorken.PDF).

[31] I. Dunietz, Phys. Lett. **B316**, 561 (1993).

[32] A. Ali, *et al.*, Phys. Rev. **D61**, 074024 (2000).

[33] A. Ali, V.M. Braun and H. Simma, Z. Phys. **C63**, 437 (1994); J.M. Soares, Phys. Rev. **D49**, 283 (1994); S. Narison, Phys. Lett. **B327** 354 (1994).

[34] F. DeJongh and M. Shapiro, *A Proposal for Observing Radiative B Decays at CDF*, CDF Note 2570; K. Kordas *et al.*, *The CDF Penguin Trigger*, CDF Note 3771.

[35] "Measurement of J/ψ and $\psi(2S)$ Polarizations in $p\overline{p}$ Collisions at $\sqrt{s} = 1.8$ TeV." T. Affolder *et al.*, Phys. Rev. Lett. **85** 2886 (2000).

[36] E. Braaten, B. Kniehl, and J. Lee, hep-ph/9911436.

Chapter 3

Run IIb Silicon Vertex Detector (SVX IIb)

3.1 Introduction

During the Spring and Summer of 2000 the CDF Run IIb silicon Working Group studied the lifetimes of all components of the CDF Run IIa silicon detectors in order to establish integrated luminosity levels that can be attained with reasonable detector performance [1]. The Working Group concluded that it was not possible to guarantee that these limits, shown in Table 3.1, can be exceeded. As a result, a substantial portion of the Run IIa detector can not be guaranteed to survive Run IIb (15 fb^{-1}) and would thus limit our ability to capitalize on the exciting physics opportunities at Fermilab before the start of LHC. In particular, there is a significant likelihood that L00, the innermost 3 layers of SVXII, and all SVXII port-cards will need to be replaced. It was also clear that the schedule for such a replacement would be driven in large part by the schedule for a new radiation tolerant SVX chip (called SVX4). A small group of engineers from LBL, Padova and Fermilab was formed and made great progress on the SVX4 chip design in the past 2 years. The first full chips are expected to be in hand during the spring of 2002. The goal for the Run IIb installation is a six month long shutdown in the first half of 2005. In order minimize the shutdown period, a complete replacement for SVXII and L00 is necessary. As discussed in the working group report, any alternative, such as a partial replacement, would require a much more extensive shutdown.

The CDF Run IIb silicon detector is designed to be a radiation tolerant replacement for the SVXII and L00 detectors that is optimized for Higgs and new particle searches while also being affordable, robust, and simple to construct and operate. To minimize development time, the design makes use of existing and tested technologies to the largest extent possible. The design presented in this Chapter represents our

Layer	Safe Lifetime (fb^{-1})	Cause of Death
L00	7.4	V_{dep}
L0	4.3 (5.6)	S/N (V_{dep})
L1	8.5 (10.9)	S/N (V_{dep})
L2	10.7	V_{dep}
L3	23 (30)	S/N (V_{dep})
L4	14	V_{dep}
L6	> 40	n/a
L7	> 40	n/a
L8	> 40	n/a
Port-cards:		
SVX-II	5.7	DOIM
ISL & L00	14.6	DOIM

Table 3.1: Safe lifetimes for each layer of SVX-II as defined in the text. In the "Cause of Death" column S/N stands for signal to noise and V_{dep} for depletion voltage.

baseline design. Some changes may be required as we learn more about the operation of the RunIIa detector. For example, between the last Technical review of the Run IIb silicon project the following changes have been made:

- The 90 deg. stereo sensors have been replaced with axial and small-angle stereo sensors.
- Layer 1 is constructed of outer layer staves significantly reducing both the cost and complexity of the project.
- Layer 1 will have axial sensors on both sides of the stave for redundant measurements in this critical region.

In addition, we are currently studying two options for the sensors on Layer 5. Under consideration are axial layers on both sides or axial on one side and an additional small-angle stereo layer on the other side. For the purposes of this document we assume that layer 5 has axial sensors on both sides, however, further study is needed to determine if double axial or small-angle information is more advantageous for Run IIb pattern recognition. The current status of those studies is presented in the next Chapter. This decision has no impact on the cost or schedule of the project. The axial and small-angle sensors are the same price. The stave construction fixtures and procedures are independent of the sensor type. A decision is only needed by the time of the order of the production sensors (currently estimated as Sept. or Oct. 2002).

3.1.1 Conceptual Design

Having established that the present SVXII and L00 will not withstand the amount of radiation that will be accumulated during Run IIb, the design of the replacement detector must address three important issues:

1. It must withstand the radiation corresponding to an integrated luminosity in excess of 15 fb^{-1} during a period of 3 years.
2. It has to be ready for installation by Jan. 2005.
3. It has to retain or improve the performance of the present device.

Parts	SVXII + L00	Run IIb
sensors	7	3
hybrids	12	2
ladders/staves	7	2

Table 3.2: Different types of parts for the SVXII, L00 and Run IIb silicon detectors.

All three of these items are addressed by the use of single sided silicon sensors. The needs of the LHC detectors at CERN have motivated a great deal of effort on the development and understanding of radiation hard silicon sensors. Studies found that single sided sensors could be designed to withstand high bias voltages and that as long as the sensors were adequately cooled, good performance could be achieved throughout the LHC, or Run IIb, operation [4]. We intend to use this type of single sided sensor for the Run IIb detector, and will actively cool the sensors to sub-zero temperatures. Similar sensors (and cooling) are already in use in L00 of the Run IIa detector. Single sided sensor technology also has the advantage of avoiding the difficulties in manufacturing and procurement of double sided sensors that were incurred during the Run IIa detector construction.

To address item 2, we have drastically reduced the number of different types of key components such as hybrids and staves (ladders in the Run IIa language). Table 3.2 summarizes the number of types of parts for the SVXII + L00 and Run IIb silicon detectors. The outer 4 layers of the Run IIb detector utilize only two types of sensor (axial and small-angle), a single type of hybrid, and account for $\simeq 94\%$ of all detector parts. In Run IIa the total number of parts was split into 6 roughly equal sets each with its own features and difficulties.

Item 2 is also addressed by keeping the existing Run IIa infrastructure for use in Run IIb. For example, the cooling and the readout are designed to fit within the Run IIa systems. We note here a few of the differences and similarities in the Run IIa and Run IIb designs. The details are presented in later sections.

The immediate implication of using single sided silicon and direct silicon cooling is an increased amount of material inside the tracking volume. Consequently, effort has been directed towards minimizing all inactive components. With respect to the SVXII (Run IIa) design, the improvements in mass are:

- Portcards and portcard cooling have been eliminated (this by itself accounts for more than 3% X_0) from the tracking volume.
- Hybrids will use a more recent materials technology enabling smaller area and less metal coverage (by a factor of two in both cases). This same technology was used for the Run IIa L00 hybrids.
- Material and measurements are more uniformly spread over a larger volume (i.e. larger radii).
- The use of intermediate strips throughout the detector provides good resolution without the price of increased readout electronics.

The result is that despite doubling the silicon contribution (by using single-sided instead of double-sided sensors) and adding cooling to the sensors, the Run IIb design is less massive than SVXII.

The mechanical design of the Run IIb detector has been optimized for ease of construction and is quite different from the Run IIa design in that only one type of stave is used on the outer 4 layers. Figure 3.1 shows an end view of the Run IIb detector. To maintain the axial tracking capabilities of the Run IIa detector, staves will have axial silicon sensors mounted on one side of a carbon fiber rohacell structure and axial or small-angle stereo sensors mounted on the other side. The use of one structural design for the outer 180 staves will significantly reduce the production time. A wedge-based geometry has the clear disadvantage of requiring different parts (detectors, hybrids, assembly and bonding fixtures etc.) for each layer. This made the construction more complex, expensive and less flexible. Details of the mechanical design can be found in sections 3.2- 3.4.

A smaller and simplified version of the Run IIa portcard (the MiniPortCard or MPC) will be used at the end of each stave on layers 1-5. To address some of the reliability issues which have become evident with the Run IIa detector, the optical components have been removed and most of the active components of the Run IIa portcard have been moved to the more accessible junction card. This reduces the mass and cooling needed and should significantly improve the robustness of the system. Our desire to use commercially available parts combined with the higher radiation environment of the Run IIb detector has independently ruled out the use of optical transmitters for the data. Copper transmission lines will be used in place of the fiber optics. Cooper lines were tested extensively in the laser test stands used during Run IIa ladder production. More details on the MPC and rest of the DAQ system are provided in section 3.5.

3.1.2 Schedule

Preparation of a detailed schedule is underway and will be presented in a separate document. However, with a planned installation date of Jan. 2005, the rough features of the schedule are clear. Based on Run IIa experience, roughly 6 months of preparation (alignment, testing, final assembly etc.) will be needed between installation of the last stave in a barrel, and having a detector ready to install at CDF. This implies that the last stave must be completed by middle of 2004. We anticipate approximately 10 months for outer layer stave production, allowing some time for ramp up. This implies that production components for the outer layers must be in hand by the middle of 2003. This is achievable if the production chips, hybrids and sensors can be ordered in the fall of 2002. It is clear from these constraints that the schedule for R&D and prototyping is very limited compared to previous projects. We have thus, at every step of the design, tried to simplify and minimize the technically challenging tasks, without compromising the performance of the detector.

Prototyping activities were initiated in 2001 (where possible) and the project is in good shape for having key components for prototype stave construction to start by the middle of 2002. The first full chips will be in hand and available for installation on hybrids and the hybrid prototyping schedule meshes well with this schedule. By July 2002, prototypes of both hybrids and chips should allow testing and evaluation to begin. Another critical component is procurement of the silicon sensors. A small prototype order of the outer layer designs has been placed so that sensors will also be available for evaluation with the chip and hybrid. Other long lead time items are the beampipe, bulkheads, L0 signal cables followed by DAQ components and power supplies.

One schedule concern is the time required to swap out the old detector and install and commission the new one. A six month shutdown period leaves essentially no contingency for installation and includes little or no time for connecting and commissioning. With the experience of Run IIa to guide us, we are developing a plan to minimize as much as possible the turn-around time for the Run IIa to Run IIb transi-

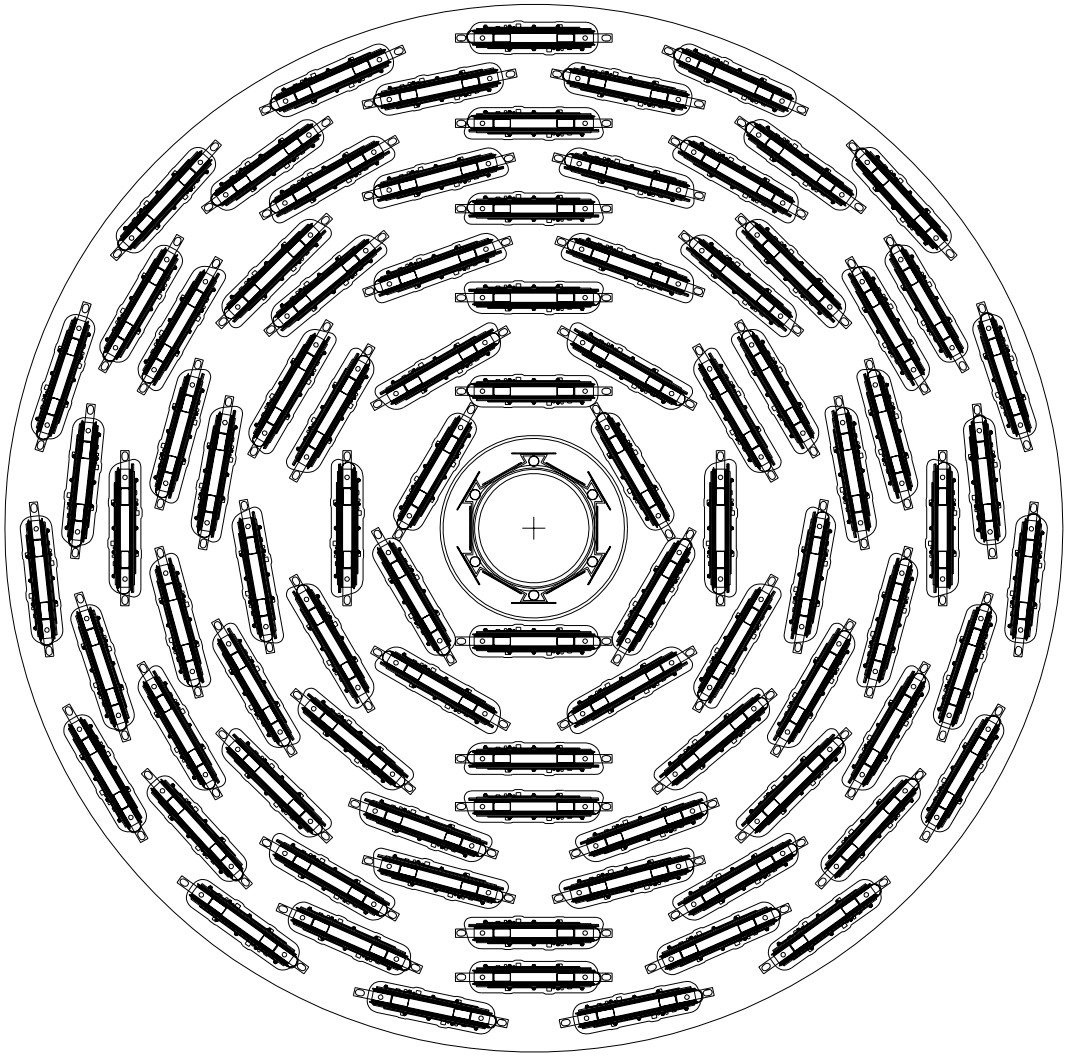

Figure 3.1: SVXIIb layout. Note that one stave design is used for the outer five layers and the innermost layer is very similar to the Run IIa L00 design.

tion.

The design presented in the following sections is the result of many studies, iterations and optimizations with input from mechanical and electrical engineers and physicists. We have based many of the design decisions on the experience of the previous silicon projects (SVX, SVX', SVXIIa, L00 and ISL). The structure of the document is as follows: section 3.2 describes the overall mechanical layout, the stave and barrel design, and alignment. Section 3.3 discusses the cooling system. The sensors and the fine pitch cables for the inner layer are described in section 3.4; section 3.5 covers the data acquisition system including the hybrids, the mother cables, the miniportcards, external cables, junction cards, FIBS and power supplies. The details of the SVX4 chip are presented in 3.6. Section 3.7 compares the material in the Run IIb design with the Run IIa detector and section 3.8 describes the descoping plan. Section 3.9 concludes with a summary of the mechanical and electrical design. The subsequent chapter is devoted to a description of the simulation efforts, analysis of Run IIa data and the expected performance of the completed Run IIb silicon detector.

3.2 Mechanical Layout

3.2.1 Overview

The Run IIb detector is designed to maintain and enhance where possible the capabilities of the Run IIa detector, while allowing for quick construction and assembly as well as flexibility in terms of descoping. The new detector has 6 layers with two barrels in z, each 66 cm long. As in the Run IIa SVX detector, the staves within a layer are arranged in a castellated pattern as shown in Figure 3.1. However, to minimize the construction time, the Run IIb design has abandoned the 12-identical wedge structure of the Run IIa detector. The Run IIa portcards (and associated cables and cooling) have been removed from the tracking volume, to minimize mass and to allow the active layers to be more evenly distributed in radius. The key feature of the Run IIb design is that the outer 4 layers use identical structural elements, called staves, to support the silicon sensors. Figure 3.2 shows an isometric view of a stave. Each stave has built-in copper-kapton bus cables and cooling tubes which are sandwiched between 6 axial sensors on one side, and 6 axial or stereo sensors on the other side. Four-chip hybrids are used to read out two sensors each and are glued on the silicon (as in Run IIa). Layers 2-4 will have axial on one side and small-angle (1.2°) stereo sensors on the other side. The axial (stereo) sensors are 40.5 (43.1) mm wide and 96.4 mm in length. Layers 1 and 5 will have axial on both sides. The modularity of the outer 5 layers in ϕ, starting from the outer layer (layer 5) is 30, 24, 18, 12 and 6. The total number of staves in the outer layers is 180. Of these, 72 are double axial and 108 are axial plus 1.2° stereo. The radial locations of the Run IIb silicon layers are given in Table 3.3. The locations of the layers in the Run IIa detector are also listed.

The innermost layer (called Layer 0) is very similar to the Run IIa Layer 00 design [8]. It is a 12-fold symmetric axial layer and uses fine pitch cables between the sensors and the hybrids. The hybrids are located outside the tracking volume. One difference is that the Run IIb L0 has only one sensor and hybrid type. These are similar to the L00 2-chip modules (L00 had both one-chip and two-chip sensors and hybrids). The L0 sensors are identical to the 2-chip L00 sensors used in Run IIa; they are 14.85 mm in width and 78.5 mm in length. Two sensors are ganged together and readout by one hybrid. The length of L0 is 12 sensors plus gaps between modules for a total coverage of approximately 96 cm.

Layer 1 must provide redundancy for the axial tracking of Layer 0, but the circumferential space is very limited. We have found that the most robust layout for Layer 1 is an outer layer stave with axial sensors on both sides. The angular coverage of Layer 1 is only 85%, but the gaps are covered by the inner staves of Layer 2 as shown in Figure 3.1.

In summary, to speed construction of the Run IIb detector, we have minimized the number of different structures to be built. There are only two types of hybrid and only three types of single-sided sensors (two on the outer layers and one for Layer 0). Table 3.4 compares SVX IIb design parameters with those of the current SVX IIa design. Simulation studies of the Run IIb layout are discussed later and are compared to the Run IIa configuration. Note that the innermost layer has moved out for Run IIb. This allows for a much simpler construction procedure for this layer without degrading the impact parameter resolution. Also, the outermost layer has moved out roughly 5 cm as a result of the elimination of portcards and the associated cables and cooling. An important feature of the Run IIb design is that the outer staves are essen-

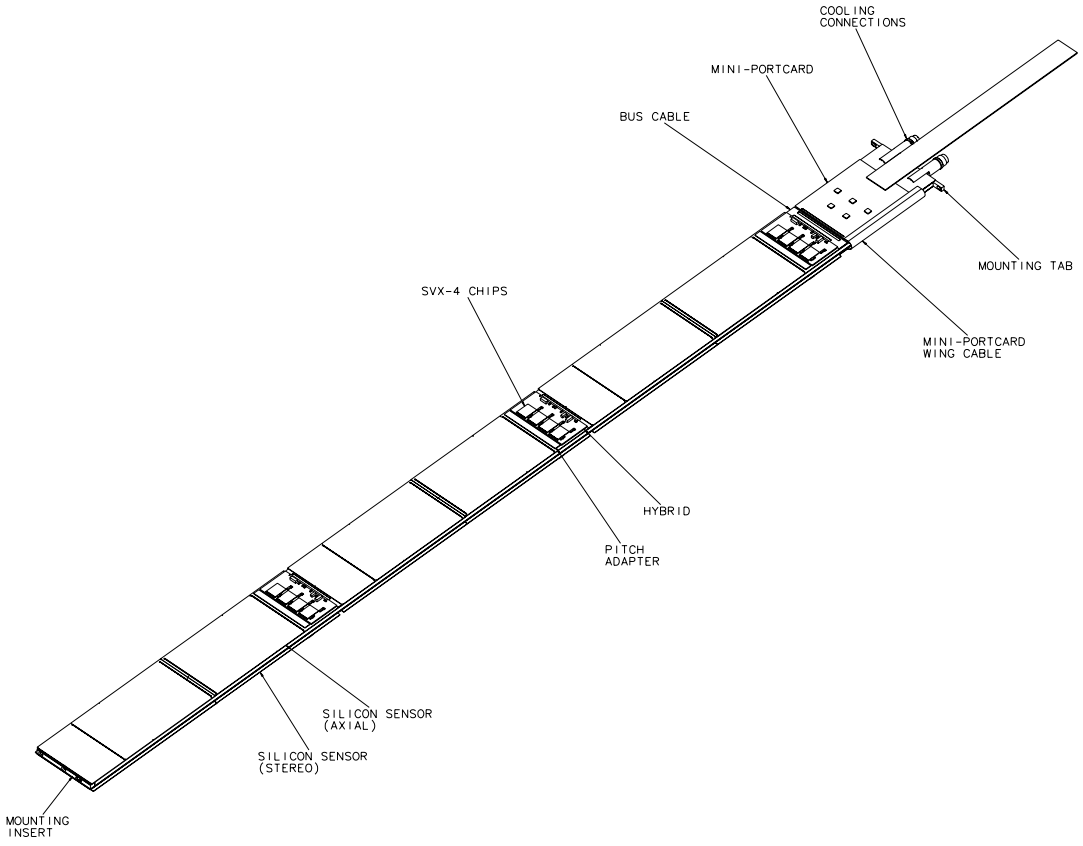

Figure 3.2: Run IIb stave design.

tially interchangeable. If further study shows that, for example, the outer layers should be rearranged, this will have no impact on the fixturing and prototyping for stave construction. This flexible design also allows a nonintrusive descoping plan which will be discussed in section 3.8.

3.2.2 Stave (ladder) Design

The detector is made up of three types of assemblies. The type used in the largest quantity is shown in Figures 3.2, 3.3 and 3.4 and is utilized in layers 1 through 5. The upper face of the stave is made up of three readout modules. Each module is made up of two axial sensors wirebonded together and a readout hybrid that is glued onto the silicon surface at one end of one sensor. The axial (small-angle) sensors are 96.393 mm long and 40.55 mm (43.10 mm) wide. The hybrid is fabricated on beryllia ceramic using thick-film circuitry (see Section 3.5). Its surface includes areas for four SVX4 chips, a wire bond field for bonding to a pitch adapter and a wire bond field used to connect the hybrid to the bus cable that passes underneath the silicon sensors. The hybrid is wirebonded down to this bus through a small gap between adjacent sets of sensor modules. A pitch adapter is glued to the silicon, next to the hybrid, and facilitates wirebonding between the SVX4 chip pads on the hybrid and the sensor pads. The bottom face of the stave is similar to the top, except that it is comprised of either axial (layers 1 and 5) or 1.2° stereo (layers 2-4) sensor modules. The hybrids used will be exactly the same on the axial and stereo sides and different pitch adapters will be used to match each sensor pad frame to the chips pads on the hybrids. Identical bus cable pass underneath the sensor modules on each side of the stave. These cables are connected at the end of the stave at the Mini-Port Card (MPC). The MPC processes the readout and regenerates the signals for transmission to the external DAQ system. It is mounted on the axial side of the stave past the end of the sensor modules. A small copper kapton "wing" cable is used to connect the bus cable on the stereo side of the stave to the MPC on the axial side of the stave.

The core of the stave itself is fabricated of carbon fiber composite skins on a foam core with a built-in cooling tube. The cooling tube is formed from 0.1mm walled polyetheretherketone (PEEK) plastic, which was selected for its ability to withstand radiation environments. It runs in a U-shaped path along the stave, having both its inlet and outlet beyond the active region of the detector. It provides cooling for the ϕ- and z-side sensor modules and the MPC.

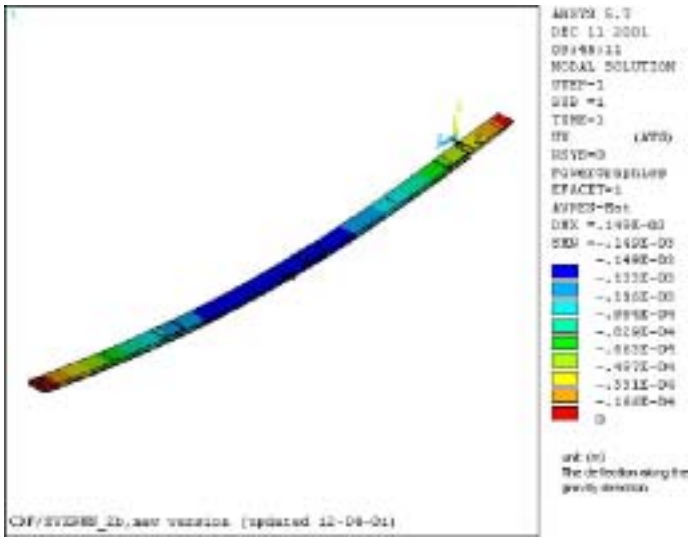

Figure 3.5: Finite element analysis of stave structure under gravity.

Stave position within the detector is registered in two locations. At the inner end of the barrel, pins extend out from the bulkhead to engage precision holes located in an Aluminum stave core insert. At the outboard end of the barrel, pins integrated into the bulkhead engage slots built into the stave core. The slots allow adjustment of the stave position within the barrel.

The emphasis on a low mass construction results in a significant sag over the length of a stave. With the staves only supported at z=0 and ±66 cm, the sag in the middle is expected to be ≈150μm. This is within the 160μm specification (see section 3.2.9). Prototype staves will be used to verify these results. Figure 3.5 shows the results of the finite element analysis of the stave structure.

The L0 configuration is very similar to the L00 detector used in Run IIa. It will be 12 fold symmetric and use sensors that are 2 chips wide (L00 alternated 1 chip and 2 chip wide sensors). A carbon fiber support structure with integrated cooling tubes will be mounted on the inner bore of each barrel and will be used to support the silicon. Six modules of two sensors each will be mounted at each ϕ location. In a module, the two sensors will be glued and bonded together and connected to a L00 type hybrid with a long fine pitch cable. The hybrids will be at $|z| >$

Description	IIb Axial R (cm)	IIb Stereo R (cm)	Run IIa label	R(cm) IIa
Layer 0 inner	2.10		L00a	1.3
Layer 0 outer	2.50		L00b	1.85
Layer 1 inner	3.50	4.00 (0°)	L0a	2.54 (90°)
Layer 1 outer	4.35	4.80 (0°)	L0b	2.99 (90°)
Layer 2 inner	5.95	6.40 (1.2°)	L1a	4.12 (90°)
Layer 2 outer	7.475	7.925 (1.2°)	L1b	4.57 (90°)
Layer 3 inner	9.525	9.075 (1.2°)	L2a	6.52 (1.2°)
Layer 3 outer	10.90	10.45 (1.2°)	L2b	7.02 (1.2°)
Layer 4 inner	12.375	11.925 (1.2°)	L3a	8.22 (90°)
Layer 4 outer	13.750	13.30 (1.2°)	L3b	8.72 (90°)
Layer 5 inner	14.750	15.20 (0°)	L4a	10.09 (1.2°)
Layer 5 outer	16.150	16.60 (0°)	L4b	10.64 (1.2°)
Bulkhead outer radius	17.5			12.75
Screen, portcards, cables				12.75-16.5
Spacetube inner radius	17.5			16.5
Spacetube outer radius	18.5			17.5
ISL inner radius	19.5			19.5

Table 3.3: Comparison of radial locations of the axial and stereo silicon layers L00, SVXII and Run IIb. Note that in SVXII double-sided sensors were used and thus the axial and stereo radii are the same.

Figure 3.3: Full end view of an outer layer stave.

Detector Parameter	SVXIIb	SVX II
Readout coordinates	r-ϕ and r-z	r-ϕ and r-z
Number of barrels	2	3
Number of staves(ladders) per layer/barrel	12;6;12;18;24;30	12
Active Stave length	59.3 cm	29.0 cm
Sensor length	9.6 cm	7.2 cm
Combined barrel length	118.7 cm	87.0 cm
Layer geometry	staggered radii	staggered radii
Radius innermost layer	2.1 cm	2.44 cm
Radius outermost layer	16.6 cm	10.6 cm
r-ϕ readout pitch	50;75;75;75;75;75 μm	60;62;60;60;65 μm
r-z readout pitch	80;80;80	141;125.5;60;141;65 μm
Length of readout channel (r-ϕ)	19.4 cm	14.5 cm
r-ϕ readout chips per stave(ladder)	2*3;24;12;12;12;24	4;6;10;12;14
r-z readout chips per stave (ladder)	12;12;12	4;6;10;8;14
r-ϕ readout channels	405,504	211,968
r-z readout channels	165,888	193,536
Total number of channels	571,392	405,504
Total number of readout chips	4464	3168
Total number of detectors	2304	720
Total number of staves (ladders)	180 (+ inner layer)	180

Table 3.4: Comparison of the Run IIb silicon and the 5-layer SVX IIa. Note that the Run IIb design includes the beampipe layer (L00 in Run IIa) while the SVXII chip and channel counts do not; the number of sensors is more than twice the Run IIa count due to the use of single-sided sensors and the addition of the beampipe layer into the total. The pitch listed for the sensors is the readout pitch. All the Run IIb sensors will make use of alternate strip readout, thus, the actual sensor pitch is half that listed in the table. In Run IIa alternate strip readout was not used for the SVXII sensors.

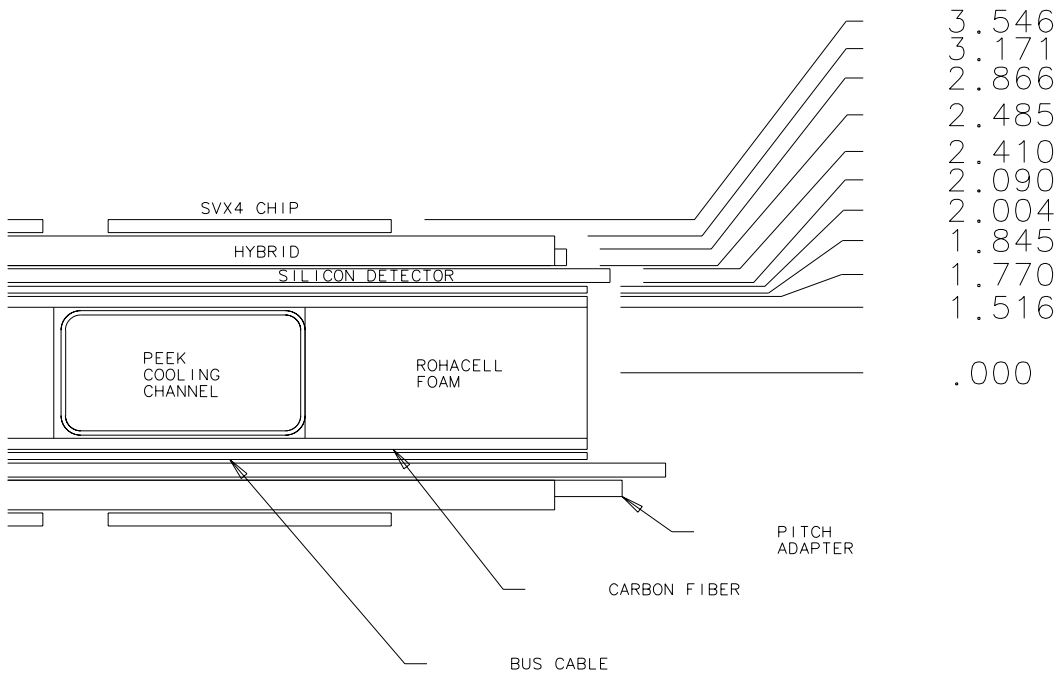

Figure 3.4: Closeup of end of a stave with dimensions (mm) of the lamination layers.

66 cm, outside of the tracking volume. To minimize material and to fit within the allowed space, the L0 hybrids will incorporate the signal regeneration function of the MPC and a separate MPC will not be required. A consequence is that each module of L0 will form one readout chain, while on Layers 1-5 all six modules on a stave are ganged together to form one readout chain. The radial location of L0 is larger than the Run IIa L00 for several reasons. First, we wished to only use one sensor and hybrid type, namely the two-chip variety and 12 two-chip sensors simply don't fit at the L00 radius. Second, the support structure of L00 was split such that the top and bottom halves were constructed separately and then mounted on the pipe. This split structure presented difficulties with the alignment. With the present design, the L0 structure is a cylinder which fits over the large flanges at the ends of the beampipe. The new design eliminates several of the challenging aspects of the L00 design.

3.2.3 Beampipe

The design of the beampipe is very similar to the original Run IIa design. The pipe is 12 feet in length, with a 20 mil wall and provides the 1" clear aperture required by the accelerator. It is constructed out of three (or five) beryllium pipe sections. In contrast to the previous pipes, we are considering a technology, where the pipe sections are drilled rather than rolled and then brazed. The drilled pipe has the advantages that it does not have a braze joint along the full length of the pipe and it also has a more circular cross section than the rolled pipe. Information on cost and schedule for delivery for each technology are being collected at this time.

3.2.4 Bulkheads

The outer barrel staves span between precision bulkheads. The bulkheads will be constructed by gluing mounting features to a flat disk. The $z = 0$ bulkheads will have holes for installation arms and small precision pins that mate with the precision holes that are built into the end of each stave. The large z bulkheads will have holes that exceed the outer dimensions of the stave by $\geq$ 1mm such that the staves can be installed through them. Figure 3.6 shows a barrel with both bulkheads and some staves. These bulkheads and the mounting fixtures establish the precision of the barrel assembly and, therefore, must be positioned to very close tolerances. We are investigating carbon fiber and beryllium for the bulkhead material. Both have a long radiation length and high stiffness. Beryllium is much more expensive and requires a very long lead-

time for machining, but may be necessary to meet the required precision.

During stave installation into the barrels, the z=0 and the outer bulkhead will be precisely aligned to each other. An inner screen will span the length of the barrel and will be glued to the inner surface of each bulkhead to maintain the bulkhead to bulkhead alignment. This structure will be supported in a rotating fixture similar to that used for construction of SVX, SVX', and SVXII. The staves will be installed through the outer bulkhead and then pinned to the z=0 bulkhead and the outer bulkhead. After stave installation is complete a cylindrical carbon fiber screen will be installed over the bulkheads and glued to them. This screen will hold the relative alignment of the bulkheads when they are removed from the rotation fixturing and will provide protection for the staves. After both barrels are complete they will be installed in a reinforced carbon fiber cylinder which spans the length to the support points on the ISL.

Figure 3.7 shows a side view of one half of the Run IIb silicon tracker, including ISL, the beampipe and the extension cylinders.

3.2.5 Spacetube

The weight of the SVX IIb detector is supported at the ends of the ISL detector using the existing kinematic mounts. The distance between these mounts is 1.95 m. A split cylindrical tube, called the spacetube, similar to that used in Run IIa will be used to span the gap between the mount points on ISL. The cylinder is split horizontally lengthwise such that the barrels can be installed from above. Figure 3.8 shows two barrels in the bottom half of the spacetube. The lower half of the cylinder will have reinforcing structures (rings and/or disks) at $z = 0$ and the $\pm$1m locations to prevent deformations of the cylinder under load. The reinforcing rings at the ends of the cylinder will also function as the structure for the beampipe supports. This open geometry leaves the detector ends accessible from above for beampipe and Layer 0 installation and for cable and plumbing dressing. Once the barrels, inner detector, and beampipe are completely installed and aligned, the top and bottom halves of the cylinder will be glued together to provide maximum stiffness and support.

The alignment of the SVX IIb silicon with respect to the beam axis is critical for the operation of Silicon Vertex Trigger (SVT). Studies for Run IIa indicated that the axis of the barrels must be aligned to within a angle of 100 μrad relative to the beam axis, corresponding to a placement of about $\pm$130 μm from end-to-end along the length of the barrels. The rigid spacetube structure will maintain the precise barrel alignment after the assembly is removed from the measurement platform and inserted into ISL.

3.2.6 Barrel Assembly and Installation

Barrel assembly will occur on a precision coordinate measuring machine. Survey balls on the outer barrel bulkheads will allow the position of the internal barrel axis to be measured without direct reference to the silicon strips. Similar fiducials on the spacetube will characterize the detector's position. The kinematic mount positions on ISL are well known from measurements during SVXII/ISL construction. The new mounts on the Run IIb space tube will be positioned such that the Run IIb detector will be aligned to ISL.

After the spacetube is closed and the alignment has been reconfirmed, the assembly will be mounted on an installation fixture. The installation fixture will support SVXIIb while the ISL, mounted on a track, slides over it. SVXIIb will then be lowered onto the ISL kinematic mount points and removed from the fixture supports. ISL junction card support ring and supports for cables and cooling tubes are then arranged such that the ISL extension cylinders can slide over them. Beampipe supports are then installed. These over-constrain the pipe, and limit the amplitude of oscillations at the middle of the pipe. This installation process was used for the assembly of the Run IIa detector.

Once the installation of SVXIIb into ISL is finished, the entire 3m long assembly is transfered to the transportation cage and carried to the CDF assembly hall. Installation into the COT proceeds directly from this fixture and will follow the same procedures which were developed for installation and removal of the Run IIa detector.

3.2.7 Alignment with the Beam Axis

After the installation into the COT is complete, the position of the Run IIb silicon detector will be adjusted by moving the combined SVX/ISL assembly. The initial position of the detectors will be determined and adjusted by referencing the beampipe position (centered with respect to the silicon) to the end

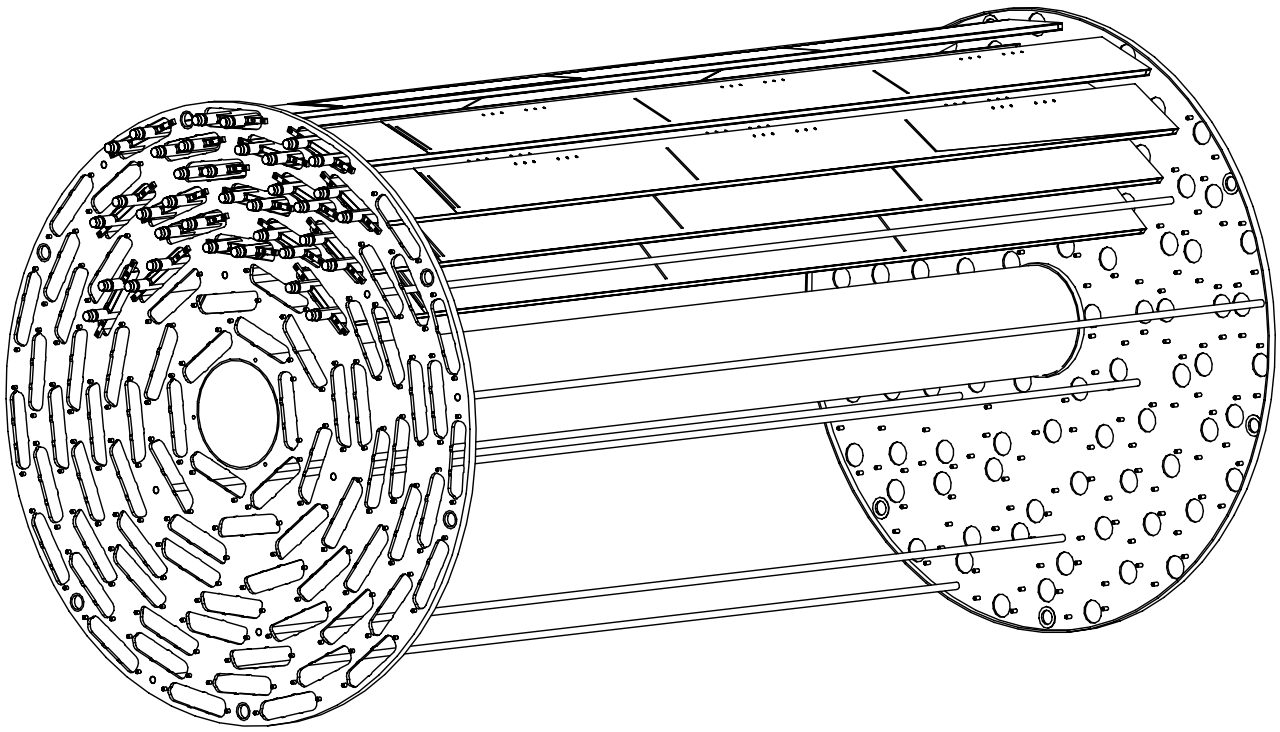

Figure 3.6: Isometric view of a barrel. Both bulkheads are visible along with a few staves. The inner bulkhead ($z \approx 0$) is on the right and the outer bulkhead is on the left. Also shown are rods connecting the bulkheads. These could be used to provide extra constraints on the bulkhead to bulkhead alignment.

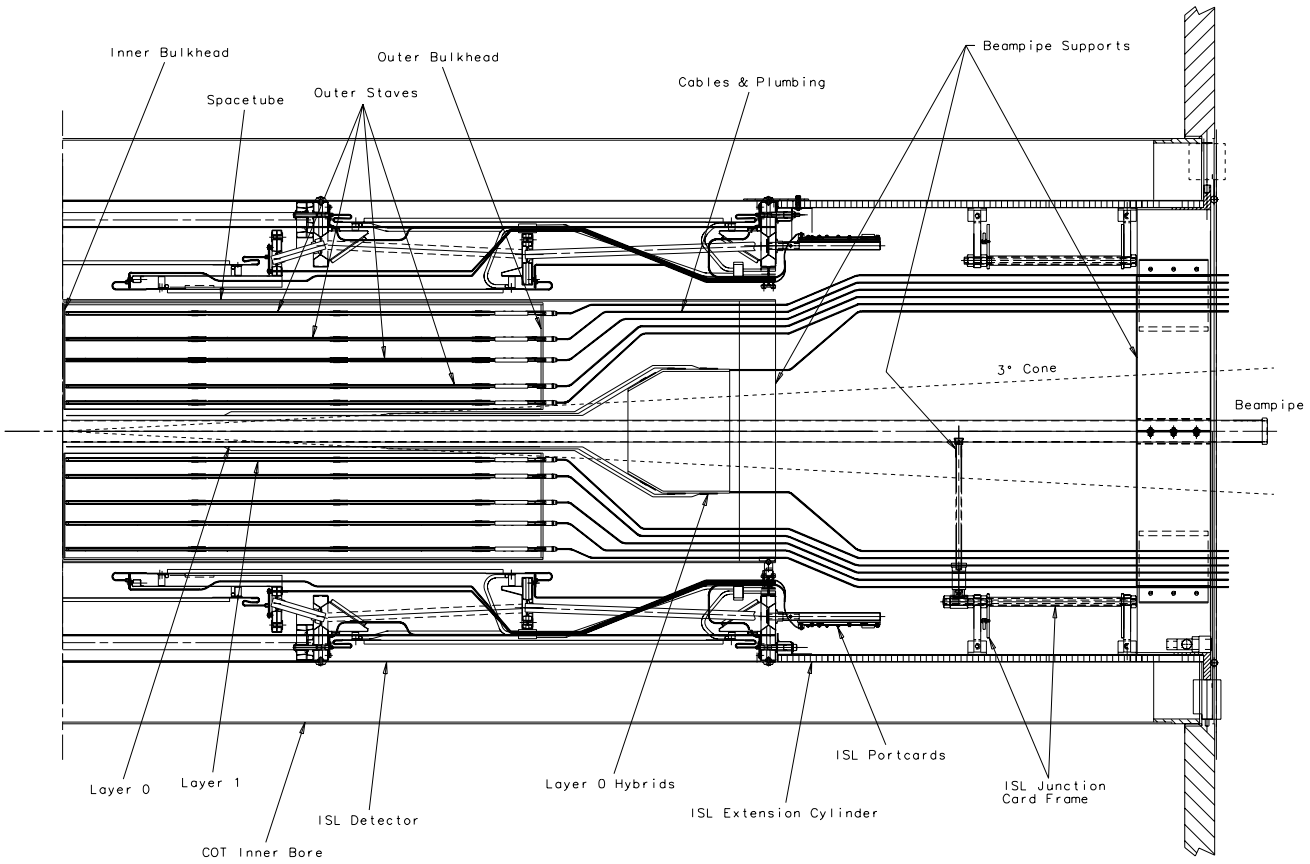

Figure 3.7: Side view of one half of the 3m long Run IIb detector. The outer bulkheads are at $|z| \approx 66$cm. The Run IIb spacetube spans the gap between the ISL mount points ($\approx \pm$ 1m). The beampipe and beampipe supports are shown along with the junction card ring and the ISL extension cylinders.

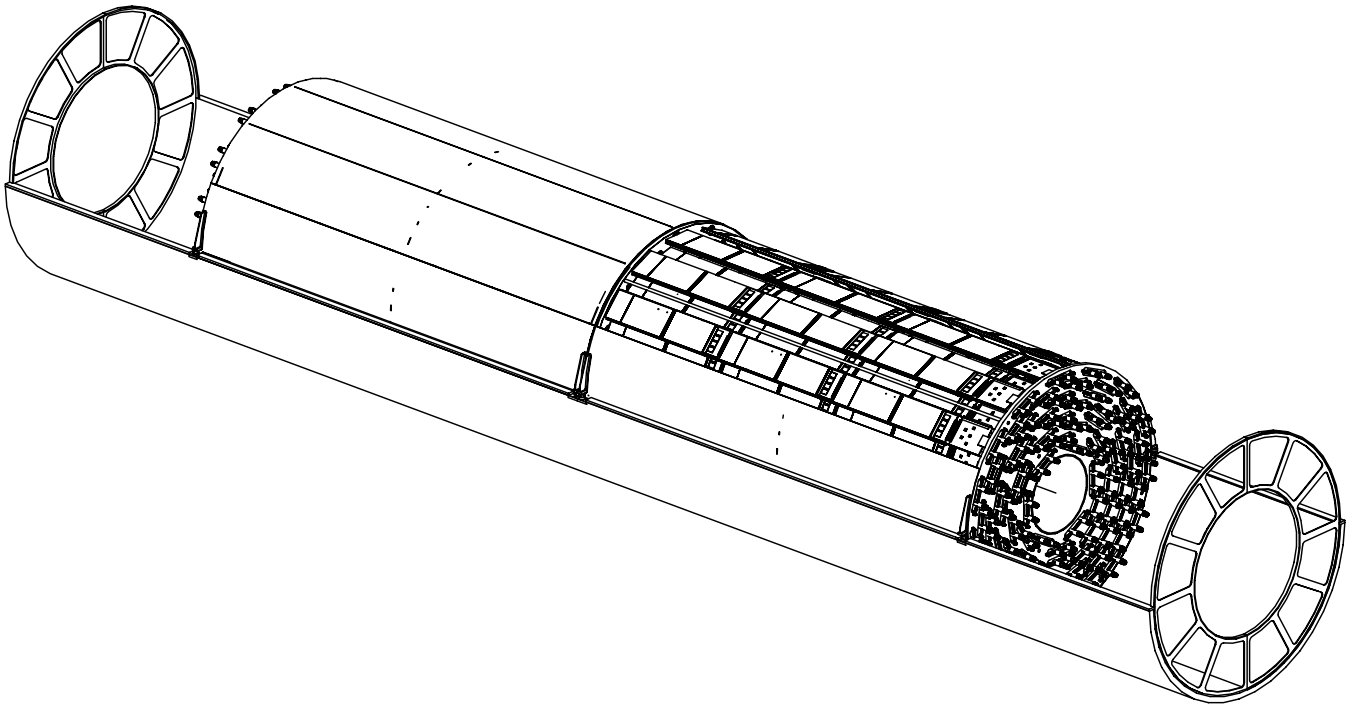

Figure 3.8: Two barrels are shown in the bottom half of the spacetube. The outer bulkheads are at $|z| \approx 66$cm. Reinforcing wheels are show at the end of the space tube. These minimize deflections of the tube and provide strain relief for cables and cooling.

flanges of the COT. Survey points on the ISL and SVXIIb can also be tied to the reference system of the CDF detector. This alignment should place the detector within 1-2mm of the correct position. The detector position with respect to the beam is precisely determined using data from the $p\bar{p}$ collisions. If need be, the detector position can be readjusted by moving either the entire tracking system (COT + ISL/SVXIIb) and thus preserving their relative alignments, or by adjusting only the position of the silicon systems. Experience with Run IIa will determine if it is possible that steering of the Tevatron beams can provide this final alignment instead of moving the detectors. In either case, as in Run IIa, beam steering will be used to maintain the position and alignment of the beams between and during stores so that adjustments in the detector position should be needed only rarely.

3.2.8 Secondary Vertex Trigger (SVT)

The impact of the present detector design on the SVT trigger has been considered. The non-wedge-based geometry presents some challenges which are not present in the Run IIa SVX detector. However, similar issues were addressed in the implementation of L00 in the SVT trigger in Run IIa. The Run IIb design is compatible with the Run IIa trigger system provided a few adjustments are made to the present SVT hardware. A minimum set of modifications have been identified which would allow the use of the L2 SVT trigger with the Run IIb detector in a fully satisfactory manner.

The number of readout chains in the Run IIb detector is compatible with the SVT system and studies have found that the expected readout times are within the window allowed for the trigger at 132 ns operation. The main issue remaining is the 12-fold ϕ segmentation of the present trigger scheme. The immediate consequence of having abandoned a wedge symmetric design is the potentially unacceptable degradation of the track fitter performance since layer radii are not always constant within a ϕ segment. This degradation of performance with the present track fitter is being assessed and will determine whether a redesign of this board is needed. The cost of a redesign is included in the baseline cost estimate.

The minimal change required to the SVT is that 12 more merger boards, identical to those presently in use, need to be added to the system. These are needed for the hits from staves which span ϕ boundaries to be distributed to two different ϕ sections further upstream. This will allow the trigger decision to proceed without the additional cost of more external connections. The current SVT crates can accommodate the additional boards.

3.2.9 Alignment

The alignment requirements for SVXII were driven by the needs of the SVT trigger and these are assumed to be the same as for Run IIa. Specifically the requirements for the barrels in the space tube are:

1. slope within ± 100 μrad of nominal,
2. transverse position within ± 250 μm, and
3. longitudinal position within ± 1 mm.
4. The deflections under full load must be stable and repeatable to ± 10 μm before, during, and after installation into the ISL.
5. The thermal stability must be better than $\pm 10 \mu$m over a 25^oC range.
6. The torsional deflection due to variations in the strain from the cable, cooling pipe and other asymmetric loads should be less than 10 μm at the mounting points of the detector.

These alignment tolerances are quite tight and are being reevaluated in light of the Run IIa data analysis. It is possible that they could be relaxed and thus could significantly reduce the time spent on stave construction, alignment and measurement in the barrels. A preliminary evaluation of the new specifications is given below.

To understand the assembly alignment requirements, we first note the difference between the construction position tolerance, which may be difficult to achieve, and knowledge of the position of a misaligned component, which may be easier to measure. The only significant restriction on the construction tolerance is given by the silicon–based impact parameter trigger (SVT). Since the track fits are done with constants which can be adjusted for each trajectory, all misalignments, once measured, can be corrected except for one case. This case arises because the trigger has only transverse information and thus knows a hit z position only within a silicon readout unit.

Therefore, within a readout unit, the strip position uncertainty as a function of z must be limited.

To provide an approximate limit on the allowed misalignments we make the following assumptions: 15μm resolution on outer layers, 9μm resolution on the inner two layers, and 1.8% momentum resolution from the external track. Fitting these parameters and allowing for the fact that the impact parameter resolution from the trigger will include a beamspot of at least 23μm, we find that the high-momentum track resolution itself may grow as much as 100% of its nominal 9μm before the total impact parameter resolution is degraded by 5%. The actual performance of the trigger will not see this full effect since the misalignment resolution will be further masked by multiple scattering.

Next we distribute the allowed misalignments, in the form of additional hit resolution, to the layers in a pattern that tends to preserve the impact parameter resolution. We allow an additional 9μm resolution to be added to the inner layers and a 13μm resolution to be added to the outer layers.

Finally, we use an RMS analysis to interpret the allowed increases in resolution as tolerances on placement of the devices. For motions in the phi measurement direction, there is no limit since these misalignments can be removed in the SVT software. For rotations about the radial axis, we find a limits of $\pm$150μrad for layer 0 and $\pm$180μrad for the other layers. This applies to each readout unit (order 18cm) individually, relative to the beamline, and with no relation to the other readout units. For radial placement limits, we consider a model where silicon placement, sag, other bows, and silicon warpage all contribute to the position of the readout unit, and the radial positions are roughly equally distributed between a maximum deviation $\pm D$ from the average radius. We find the following limits on D for layers 0 to 6: 66, 67, 54, 85, 122, 160, 200μm.

This style of analysis does not address questions such as pattern recognition or χ^2 degradation, or tails of the distributions, which may not follow RMS rules due to, for example, correlated misalignments.

In the consideration of alignment for offline reconstruction there are no assembly tolerances, only guidelines for the measurement of component positions. This approach is possible since in the offline environment any known misalignment can be corrected once we have full knowledge of the track position. A second point is that, historically, the mechanical assembly measurements of detectors have disagreed with the tracking alignment in some respect, and when they do, the track-based measurements are given the final word. A third observation is that with enough time and sufficient effort of collecting and analyzing special data sets, the silicon detector alignment can be completely aligned using tracks. We conclude that, with respect to offline, the construction alignment measurements are a matter of degree of confidence, insurance, or convenience rather than tolerances.

A feature of the Run IIb design is that the staves will be supported off the end of the silicon wafers. It should thus be possible to view the entire sensor area of the staves when they are installed in the barrels and to measure their horizontal positions to better that 10 μm in the barrel reference frame (for Run IIa only the middle 15cm of a 30 cm stave was visible). Another feature of the IIb design is that some of the layers are upside down compared to the other layers (the axial layer is on the inside rather than the outside). It will thus be possible to directly measure the Hall effect drift by taking a small amount of data with and without the magnetic field. In Run IIa this is possible only in the ISL.

In Run IIa the axial and stereo views are on the same sensor and thus very precise relative alignment was possible. In Run IIb the two views on a stave are separated by the about 5mm. Although it is not critical to position the axial and stereo sensors extremely precisely to each other, measurement of their relative positions at the level of 15μm should be possible and would be a significant time savings in commissioning.

3.2.10 Position Monitoring

A Rasnik (or similar) system for monitoring the overall position of the barrels can prove useful in detecting the large unexplained shifts observed in most detectors. Position monitors will be located on the barrels and plug directly into the existing Run IIa system.

3.3 Cooling and Gas systems

The silicon should be maintained below the temperatures listed in Table 3.5 for nominal operating conditions. In Layer 0 we expect roughly a 10 deg. difference between the coolant temperature and the temperature of the sensors and thus we anticipate the coolant temp for Run IIb will be need to -15 deg. C to achieve the goals in the table. Thermal runaway was

Layer	Temp. (deg. C)
0	-5
1	-5
2	+10
3	+10
4	+15
5	+15
6	+15

Table 3.5: SVX IIb temperature specifications

	Heat Load per Stave (W)
SVX4 chips (24)	9.6
Convection	4.2
MiniPC	2.5
Leakage (6 cm)	1.6
Total per stave (W)	18.3
Total Layers 2-5 (W)	3240
Run IIa SVX Detector Total(W)	2800

Table 3.6: SVX IIb Detector Heat Load

a serious issue for the thermal design of the SVXII detector [3] where center silicon sensors in a barrel were not well-coupled thermally to the cooled bulkheads. Available heat transfer paths ran through either wirebonds, foam, or Nitrogen gas. Internal heat generated due to leakage current caused by radiation damage is therefore hard to remove and it leads to higher silicon temperatures. Since the amount of leakage current increases significantly as the temperature increases, a positive feedback system exists, potentially leading to a catastrophic thermal runaway condition if cooling is insufficient.

For the SVX IIb detector, the design integrated luminosity of 15 fb^{-1} is much higher than for SVXII, so the leakage current will be much higher. Having silicon sensors that are only loosely coupled thermally to the cooling system is simply not a design option. Each stave must therefore be equipped with its own cooling channels to couple the sensors to the coolant more directly. In this way, the issue of thermal runaway has been effectively eliminated. The nominal heat load anticipated within the detector is shown in Table 3.6. These numbers assume 400 mW per SVX4 chip, 0.27 W per sensor for internal heat generation after 30 fb^{-1} integrated luminosity ($40\mu A/cm^2$, 15^oC operating temp, 250 V depletion), 0.5 Watts for each transceiver (5) on the mini-PCs, and convection with a 0^oC environment when the fluid temperature is -15^oC. Note that the SVX4 chip is expected to use less power than the 420 mW SVX3D chip since the operating voltage is 2.5V instead of 5V.

The existing SVXII cooling system will be used for cooling the Run IIb detector. The Run IIa system is designed to operate at -10°C with 30% ethylene glycol by weight in water, which has a freezing point of -14°C. However, in order to achieve the specified silicon operating temperatures for layer 0 in Run IIb, the system will have to operate at a colder temperature, nominally -15°C. Therefore, the ethylene glycol percentage will be increased to 43% by weight, yielding a freezing point of about -25°C. This would allow operation of the cooling system down to approximately -20°C.

As in SVXII, the cooling system is designed to operate below atmospheric pressure in the detector region. Therefore, if a leak in the system were to occur, the coolant, being under a partial vacuum, will not leak into the detector environment. The gas system for the detector will provide a continuous gas flow of nitrogen at $\approx$ 200 scfh to the detector volume. This dry gas supply keeps the silicon volume slightly over atmosphereic pressure and prevents condensation. To prevent the gas from adding heat to the system, it will be cooled near its injection region by means of a compact fluid-to-gas heat exchanger integrated into one of the plumbing return lines. This will cool the gas to nearly the coolant temperature. The gas system will be monitored to prevent impurities from entering the system.

3.3.1 Stave Cooling

A total of five inlet/outlet plumbing access slots per end of the CDF detector are currently in use for SVXII+L00 and will be available for SVX IIb. One slot will be devoted to cooling L0 and L1. The remaining 4 slots will be manifolded to provide cooling to the staves in layers 2-5. The end of the cooling channels in a stave will have aluminum fittings glued to the carbon fiber structure. Flexible tubing, similar to that used in Run IIa, will be attached to the aluminum fittings. These tubes will either attach to another stave (connecting them in series) or to a man-

ifold. The cooling for Layer 0 sensors is embedded in the carbon fiber support structure as in the Run IIa L00. Cooling will also be provided to the hybrid support structure located off the ends of the L0 sensors.

A finite element thermal model has been developed to investigate the temperature trends in the silicon for the stave type used in layers 1 through 5. Temperatures in layer 0 silicon have not yet been studied in detail. Figure 3.9 shows the results of the modeling where a coolant temp of -15°C is assumed. The maximum temperature in the sensor occurs underneath the readout hybrid, as the SVX4 chips are the primary heat source in this region. Heat generated in the chips is spread through the beryllia hybrid substrate, which has a very high thermal conductivity. It is conducted through the adhesive to the silicon, where it is spread further, and then conducts down through the bus cable and adhesive layers to the composite skin on the stave core structure, which is constructed from high-conductivity carbon fiber. The heat is then picked up by the cooling channels running axially through the stave core. Silicon sensors without hybrids mounted on top of them have very small heat loads and are therefore maintained close to the coolant temperature. The warmest location is on the hybrid at the outer end of the stave. The heat from the other hybrids can dissipate in two directions along the stave while the heat from end hybrid is trapped on one side by the presence (and heat) of the mini portcard. The warmest portion of the stave is 0°C with a coolant temperature of -15°. In terms of radiation damage, the important number is the average temperature over a strip. The models indicate that the axial modules have average temperatures of -10°. The shortest small-angle strips directly under the hybrid end up with an average temperature of -4°C. These are well below the specifications in Table 3.5 because the operating temperature of the chiller is driven by the needs of the innermost layer.

The grouping of the staves into cooling circuits is driven by pressure drop restrictions for each cooling supply slot. To minimize the tubing at the end of the staves, one would like to connect together the maximum number of staves into one cooling circuit. However, to keep the system at subatmospheric pressures inside the detector volume, the allowed pressure drop within the detector cooling circuits in 4.5 psi. Figure 3.10 shows pressure drop versus flow rate for the configurations with 1, 2 or 3 staves connected in series. Lower flow rates result in larger difference between

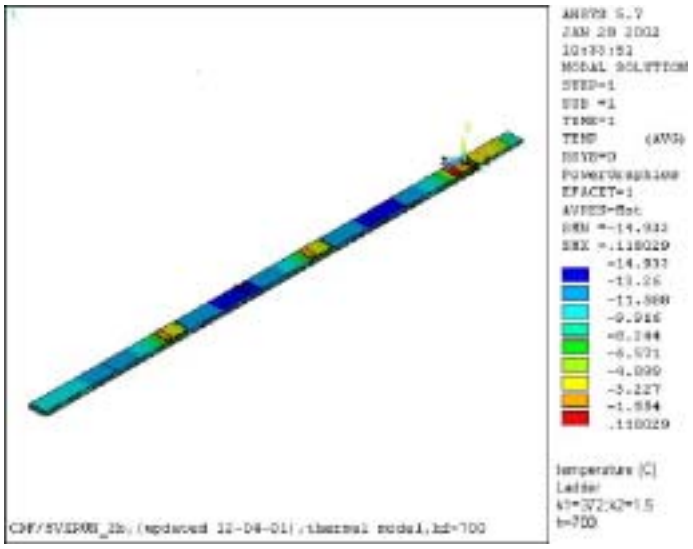

Figure 3.9: Results of finite element analysis of stave temperatures.

the inlet and outlet temperatures of the coolant. Figure 3.11 shows the pressure drop for the cases with 1, 2, and 3 staves connected in one circuit. With 3 staves connected in series, and a flow rate of 0.24 lpm, we are within the allowed total pressure drop, and the change in the coolant temperature in the 3-stave circuit is 4.3°C, or 1.4°C/stave.

As indicated above, the Run IIb design is much less sensitive than the Run IIa device to problems associated with thermal runaway resulting from radiation damage in the sensors. The effect of integrated luminosity was investigated by looking at the predicted silicon temperature in layer 2 at the beginning of the run and after 30 fb^{-1}. Only a very small difference (< 1 deg.) in the predicted temperatures was found, demonstrating that internal heat generation resulting from leakage current is not a thermal runaway concern with the Run IIb design.

3.4 Sensors and fine-pitch cables

3.4.1 Radiation damage

Silicon detectors are damaged by radiation primarily through displacement of silicon or impurities from their lattice sites (bulk damage). The other form of damage, often referred to as surface damage, is the main mechanism responsible for IC performance degradation but it has little impact on silicon detectors since their active region is mostly in the bulk away from the passivating silicon dioxide layer. As a

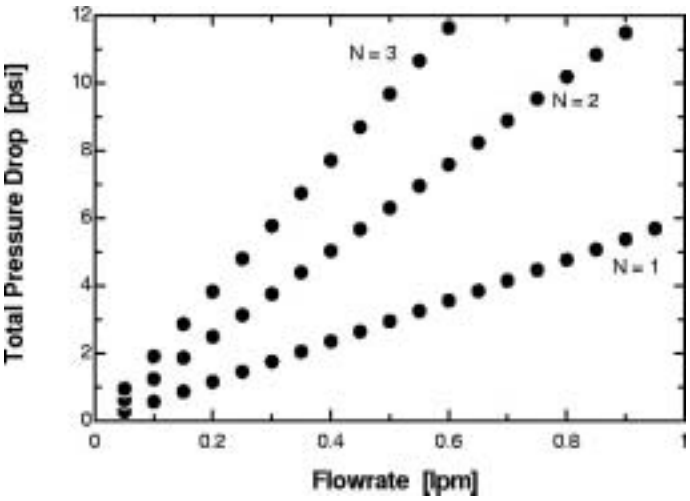

Figure 3.10: Predicted pressure drop versus flow rate for 1, 2 and 3 staves ganged in series.

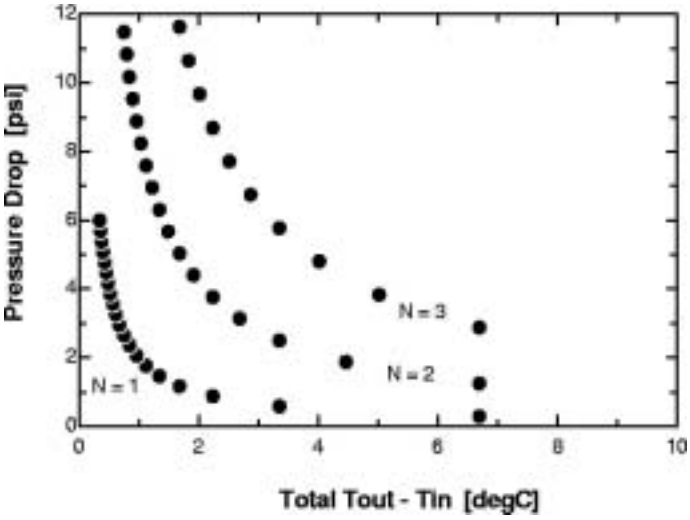

Figure 3.11: Pressure drop versus inlet-outlet temperature difference.

Period 2001	Feb-May	May-Oct.
Proton Beam (10^{19})	0.070	1.56
Pbar Beam (10^{19})	0.0082	0.137
Proton Losses (10^{9})	15.3	40.9
Pbar Losses (10^{9})	2.0	10.2
Del. Luminosity(pb^{-1})	0.058	10.7

Table 3.7: TLD exposure statistics

first approximation this mechanism can be neglected since the sensors we are proposing for the Run IIb silicon detector are single-sided p^+/n. As a result of bulk damage, silicon detectors are subjected to two main mechanisms:

- increase in leakage current and thus in the overall noise
- substrate type inversion (i.e. from n-type to p-type) which affects the depletion voltage.

3.4.1.1 Run IIa Radiation Measurements

The radiation field inside the tracking volume is measured using thermal luminescent dosimeters (TLDs) placed at 145 separate locations. During the first 9 months of Run IIa the TLDs were harvested twice. The first period from February to May was dominated by beam studies and proton losses. The second period from May to October and was dominated by proton-antiproton collisions. Table 3.7 summarizes the two exposures. Figure 3.12 shows the pattern of ionizing radiation based on measurements at two radial distances from the CDF axis as a function of the position along the axis. Protons enter from the left. In this figure, we've separated the contributions from collisions (top) and losses (bottom) using the prescription:

$$D_1 = C_1 * d_{lum}(\frac{Rad}{pb^{-1}}) + L_1 * d_{loss}(\frac{Rad}{counts}) \quad (3.1)$$

$$D_2 = C_2 * d_{lum}(\frac{Rad}{pb^{-1}}) + L_2 * d_{loss}(\frac{Rad}{counts}) \quad (3.2)$$

where D_i are the measured doses on the TLDs, C_i are the collisions (luminosity in pb^{-1}) and L_i are the losses (counts) measured in the Feb-May (i=1) and the May-Oct (i=2) periods. These two equations are solved for d_{lum} and d_{loss} and the results are plotted in Figure 3.12.

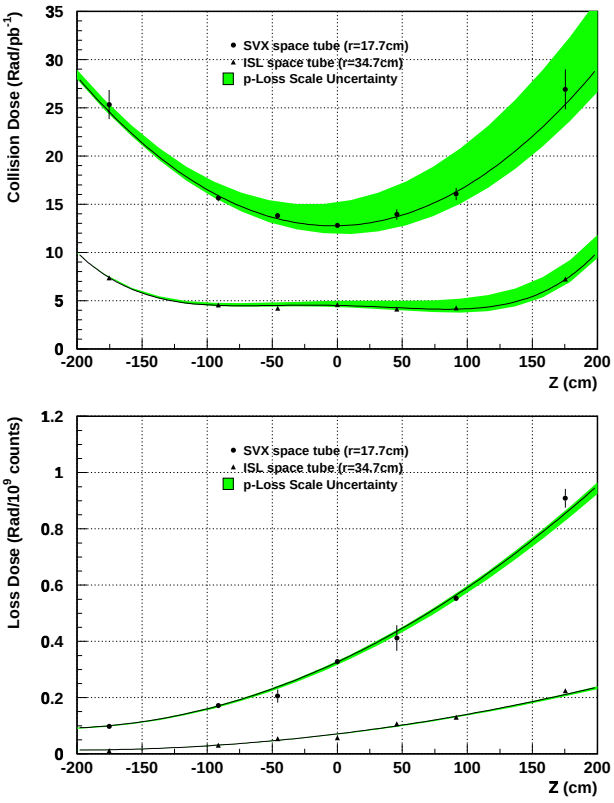

Figure 3.12: Radiation measurements and fits to Run IIa data. Ionizing radiation dose from collisions (top) and proton losses (bottom) observed by TLDs placed in the tracking volume. The data in the plots were derived from two exposures in 2001.

3.4.1.2 Leakage Current

The leakage current is extremely sensitive to temperature, doubling every $\simeq 7^o$C. It is the junction reverse saturation current and is proportional to the silicon volume considered. The generation/recombination model predicts the following dependence of the leakage current on temperature:

$$\frac{I_{leak}(T_1)}{I_{leak}(T_2)} = \frac{T_1^2}{T_2^2} \cdot e^{[\frac{-E_g}{2k}(\frac{T_1-T_2}{T_1 T_2})]}; \qquad (3.3)$$

where T is the temperature in Kelvin, $E_g = 1.12\ eV$ is the silicon energy gap and k is the Boltzmann constant. An intense research effort over the past few years (motivated by the LHC experiments) found that the increase of leakage current with radiation is linear and is independent of the particular substrate or detector fabrication process. It is thus possible to assign a global constant to the leakage current increase with radiation:

$$I_{leak} = \alpha \cdot Volume \cdot \phi\ ; \qquad (3.4)$$

where α is the leakage current damage constant at 20^oC, Volume is the silicon volume considered and ϕ is the radiation damage fluence in 1 MeV equivalent neutron$\cdot cm^{-2}$. Detectors subjected to radiation damage exhibit an increase of leakage current which decays with time after irradiation (annealing effect) with a temperature dependent time constant. Consequently the leakage current damage constant will depend on the time and temperature history of the detector. For detectors used in a collider, the damage rate is always rather low compared to the annealing time constant and we can assume that complete annealing occurs during their operation. In this case we can use an α constant of 3.2 10^{-17} A/cm. Since our silicon detectors are AC coupled there is no direct path for the leakage into the readout chip preamplifier inputs but rather its effect is seen as a noise increase. The increase in noise is independent of the intrinsic readout chip noise and needs to be added to the latter in quadrature. Since the functioning of the SVX4 chip is based on the double correlated sample and hold concept, the noise associated with the leakage current can be shown to be:

$$ENC_{I_{leak}} = \frac{1}{\sqrt{q}} \cdot \sqrt{I_{leak} \cdot \frac{x - F(x)}{F(x)^2}} \qquad (3.5)$$

$$x = \frac{T_{int}}{\tau} \qquad (3.6)$$

$$F(x) = (1 - e^{-x}) \qquad (3.7)$$

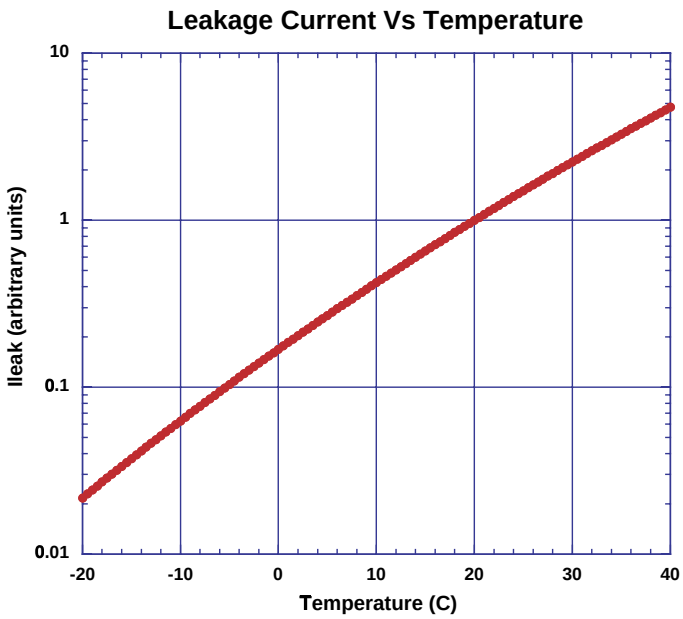

Figure 3.13: Relative variation of leakage current with temperature.

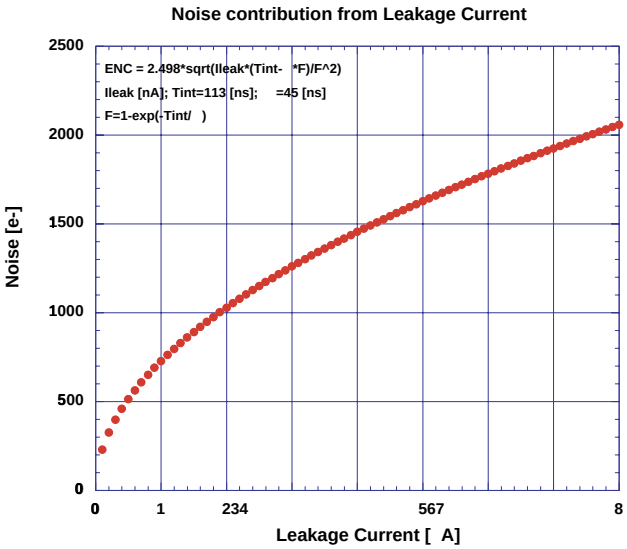

Figure 3.14: Noise (in electrons) vs Leakage current.

where q is the electron charge, T_{int} is the integration time and τ is the preamplifier rise time.

Figure 3.14 shows the component of the noise from leakage current as a function of the leakage current itself assuming $T_{int} = 113ns$ and $\tau = 45ns$. There are two handles to limit the leakage current: one is the temperature and the second is the silicon strip volume itself. In practice, though, the strip volume is defined by other considerations (resolution, occupancy, ease of fabrication etc.) and temperature remains the only control. Figure 3.13 shows the relative variation of leakage current with temperature with the arbitrary reference choice of 20^oC as the unit value. For example, lowering the temperature from 20^oC to -5^oC makes the leakage current go down by an order of magnitude. The silicon operational temperature is then set by the amount of increased noise that can be tolerated at any given radius for any type of detector (i.e. a given baseline noise and a given strip volume).

3.4.1.3 Depletion voltage

While the increase of leakage current with radiation damage is a very well understood (at least macroscopically) effect, much less so is the depletion voltage variation. This is mainly due to the fact that the donor removal rate and acceptor introduction rate (responsible for the variation of the effective dopant concentration N_{eff} and hence for the depletion voltage) are complex mechanisms, the magnitude of which depends upon many parameters such as temperature, initial resistivity, initial concentration of various impurities, type of radiation, and even detector production processes. A further complication is that damaged bulk is subject to two types of annealing, first a beneficial annealing and then a reverse-annealing which, if not controlled, will increase the initial damage by about a factor of 2. Fortunately the reverse annealing plays a role only after considerable damage has been done (in practice only after type inversion) and can be minimized by keeping the silicon at a temperature below 5^oC. Neglecting the reverse annealing effect, we can model the variation in depletion voltage using the simplified formula:

$$\Delta N_{eff}(\Phi) = N_{C0}\, e^{-c\Phi} + g_C \cdot \Phi \; ; \qquad (3.8)$$

$$V_{depletion} = \frac{q}{2K_S\epsilon_0} \cdot d^2 \, |N_{eff}| \; ; \qquad (3.9)$$

where N_{eff} is the effective dopant concentration, Φ is the radiation fluence, N_{C0} in the initial effective doping concentration, c is the donor removal rate, g_C is the acceptor introduction rate, d is the silicon thickness, q is the electron charge, K_S is the silicon dielectric constant and ϵ_0 is the vacuum permittivity. Table 3.8 shows the values used for our calculations and Figure 3.15 shows the predicted depletion voltages for

Parameter	Value	Unit
K_S	7.6610^{-8}	$V \cdot cm$
N_{C0}	2.510^{12}	cm^{-3}
c	2.010^{-13}	cm^2
g_C	1.7710^{-2}	cm^{-1}
d	3.010^{-2}	cm
Φ	2.210^{13}	$1\ MeV\ eq.\ n \cdot cm^{-2}$ per fb^{-1} *at* $1\ cm$

Table 3.8: Values of the parameters to determine the depletion voltage.

the three innermost layers as function of luminosity. In this Figure we applied a safety factor of 1.5 to the predicted dose.

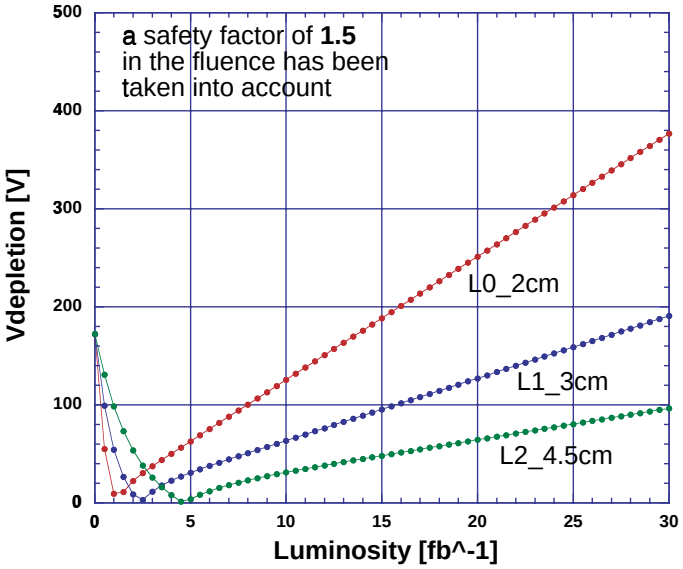

Figure 3.15: Predicted depletion voltages as a function of delivered luminosity. A safety factor of 1.5 in the expected dose has been taken into account.

3.4.2 Sensor Specifications

In this section we give a brief technical description of the sensors that will be used for Run IIb. We intend to make use of R&D performed for the LHC[4] experiments and to take advantage of the recent experience with the construction of the Run IIa silicon detectors[5, 6]. To minimize the cost, all sensors will be fabricated on 6" wafers[7] with at least two sensors per wafer. The specifications for the substrates are listed in Table 3.9. The choices of the substrate characteristics are driven by mechanical constraints as well as by radiation hardness. The specified wafer orientation has been proven to withstand fluences up to $4X10^{14}$ p/cm^2 without any change on the total capacitance of the strips [4]. The high resistivity substrate will prolong the lifetime of the sensors by delaying high voltage operation.

Parameter	Specification
Thickness	320 μm $\pm$ 15 μm
Wafer diameter	6 *inch*
Wafer type	*n*-type
Wafer orientation	$< 100 >$
Wafer resistivity	1.3 to 3.3 $k\Omega$-cm
Warp	$< 100\mu m$
Polish	Mirror finish on Junction side Ohmic side optional

Table 3.9: Properties of the wafers

Many characteristics are common to all detectors regardless of layer or stereo angle. All sensors are *n*-type, single-sided, AC coupled, poly biased silicon microstrip detectors with intermediate strips. As already described, the sensors have to withstand high radiation fluences. Consequently it must be possible to operate the sensors at voltages exceeding 500 V. Such results have already been achieved for Layer 00 in Run IIa. Figure 3.16 shows the breakdown voltage for all the Layer 00 sensors produced by *Hamamatsu*. The cut at 500 V still allows for a very high yield. Similar results have been achieved with other vendors like *ST Catania*[5] and *Micron Semiconductor L.t.d.*

3.4.2.1 Axial and 1.2° stereo sensors

For the innermost layer the sensors will be identical to the Layer 00 sensors[5]. The outer layer sensors are described here. Given the sensor thickness, the amount of signal collected is fixed, but the noise is strongly dependent on the sensor design. The feature sizes define the magnitude of the total capacitance of each strip which is linearly correlated with the noise performance. The total capacitance of microstrip detectors is well parameterized by formula 3.10 [4].

$$C_{tot} = (0.83 + 1.67\frac{w}{p})pF/cm \qquad (3.10)$$

A w/p (width/pitch) of 0.2 results in a capacitance

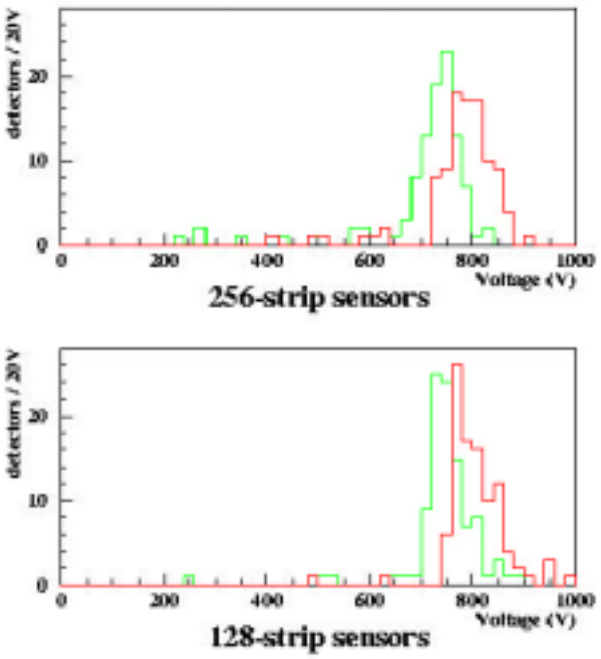

Figure 3.16: Breakdown and operational voltages of Layer 00 Hamamatsu sensor.

per unit length of 1.16 pF/cm. Strips as long as 34 cm can then be read out by a single electronic channel without compromising the initial signal over noise. The limit on signal to noise is discussed in Section 3.6, and corresponds to 40 pF. The set of specifications for the outer axial sensors is reported in Table 3.10.

3.4.3 Inner Layer Lightweight Cables

To minimize the scattering material in the first measurement layer, the L0 construction will follow the design of the Run IIa L00 detector. The analog signals from the L0 silicon detectors are read out through lightweight cables to hybrids located outside the tracking region ($|z|$ >50cm). The material of the hybrids, chips and associated cooling are thus outside the tracking volume. A concern with these long cables is noise pickup and increase in the readout capacitance could potentially degrade the system performance. Studies with the L00 detector are in progress and the noise issues look tractable.

The cable design is essentially the same as that of L00. The pitch of the trace lines is 50 μm to match the readout pitch of the sensors. In order to reduce the inter-trace capacitance, the width of the cables expands by a factor of two for most of its length. Two overlapping cables are used for each sensor pair and they pass over the top of the silicon sensors.

The lightweight cables for Run IIa L00 were fabricated at CERN. The same CAD layout file has been transferred to a private company, KEYCOM Co.[9], to evaluate the production feasibility. KEYCOM has experience making similar lightweight cables for the Belle SVD. The cable base is 30 μm thick kapton where copper is evaporated and then plated to a thickness of 5 μm. Although we found some technical problems in the first products, the trace widths are not well controlled resulting in some breaks and bridges, optimization of the pattern and use of glass masks should solve these problems. Further R&D studies are underway, and experience with the current L00 cables will be taken into account as much as possible. In particular, the issue of noise pickup will be addressed.

Once quality cable production is established, visual inspection should be sufficient for quality assurance. The company will perform visual inspection on every cable. Small bridges could be repaired using a laser: passivation with enamel is foreseen to protect against discharges initiated from such irregular surfaces and to maintain quality for a longer term. The surfaces of the bonding pads are gold plated with nickel plating underneath. The thicknesses will be optimized through wirebonding tests. The electrical performance, such as inter-trace capacitance and trace resistivity will be tested on a sampling basis.

3.5 Data Acquisition

3.5.1 Introduction

The Run IIb silicon data acquisition will re-use most of the Run IIa system. The complete DAQ system was designed for Run IIa and is described in the Run IIa TDR [3]. Here we only describe new components needed for Run IIb. The changes from the Run IIa system are driven by changes in the chip and the high radiation environment of Run IIb. The SVX4 chip, as discussed in section 3.6, with the new 0.25μm technology will operate with 2.5V rather than the 5V of the SVX3 chip. This fact, combined with the new detector geometry, requires the development of new hybrids (see section 3.5.3). In addition, studies by the Run IIb working group [1] found that the Digital to Optical Interface Modules (DOIMS) on the SVXIIa portcards [10] were not sufficiently radiation hard to survive the Run IIb luminosities. These two

Parameter	Specification
Active area dimensions	38.48 x 94.262 mm^2
Overall dimensions	40.55 x 96.392 mm^2
Strip pitch	37.5μm
Readout pitch	75μm
Number of strips	1024
Number of readout strips	512
Depletion Voltage	120 to 250 V
Biasing scheme	Poly resistor on one side
Poly resistor values	1.5 $\pm$ 0.5 MΩ (< 10% variation within a sensor)
passivation	SiO_2 0.5-1 μm thick
Implant strip width	9μm
Implant depth	$> 1.2\mu m$
Doping of implant	$> 1x10^{18} ions/cm^3$
Width of Aluminum strip	15μm
Thickness of Aluminum strip	$> 1\mu m$
Resistivity of Aluminum strip	$< 30\Omega cm$
Coupling capacitor value	$> 12pF/cm$
Coupling capacitor breakdown voltage	$> 100V$
Total sensor current at $T = 20°$ C and 500 V	$< 50nA/cm^2$
Interstrip resistance	$> 1\ G\Omega$
Total interstrip capacitance	$< 1.2pF/cm$
Bad channels	< 1% (No more than 5 per sensor)

Table 3.10: Sensors specifications for the outer axial layers

items and their associated ramifications call for a new Port Card. It is very difficult to obtain rad hard replacements for the DOIMs without substantial effort and the associated schedule delay and cost. As a result, we have chosen to use copper cables to carry the data from the portcards to Fiber Transition Modules (FTMs). The associated modifications to the FTMs are discussed in section 3.5.7. A block diagram of the new sections of the Run IIb DAQ system is shown in Figure 3.17.

For Run IIb new portcards and junction cards are being designed. Most components of the Run IIa portcard will be transferred to a new junction card leaving only transceivers behind on the new miniportcard (MPC). As shown in Figure 3.2, an MPC will be at the end of each stave and will be of minimal mass. The junction card, now called the junction portcard (JPC), will be moved outside the bore of the COT, to the face of the central calorimeter, where the COT repeater cards are mounted. The radiation dose in that region is small enough that off-the-shelf components can be used.

The active components on the new JPC's will require cooling. Sufficient cooling is available at their proposed location. The cooling required by the MPC is significantly reduced compared to the Run IIa portcards. It will be supplied by the lines which also cool the hybrids and the silicon sensors. The ISL portcards and junction cards will not be changed for Run IIb since ISL will still have SVX3 chips and they are located in a lower radiation environment than the SVXIIa portcards.

More information on the new MPC can be found in section 3.5.4. Section 3.5.5 describes the new JPC and section 3.5.6 discusses the cables which connect the MPC to the JPC and the JPC to the FTMs.

3.5.2 Readout times

The time available to read out the axial sensors is limited by the bandwidth of the trigger. The silicon vertex trigger (SVT) must produce a decision in less than 20 μsec on average for deadtimeless operation at a Level 1 accept rate of 50 kHz. The processing time of the trigger is about 10 μsec, leaving ~10 μsec for readout and digitization of the $r-\phi$ data. The stereo data is read out after the $r-\phi$ producing an additional

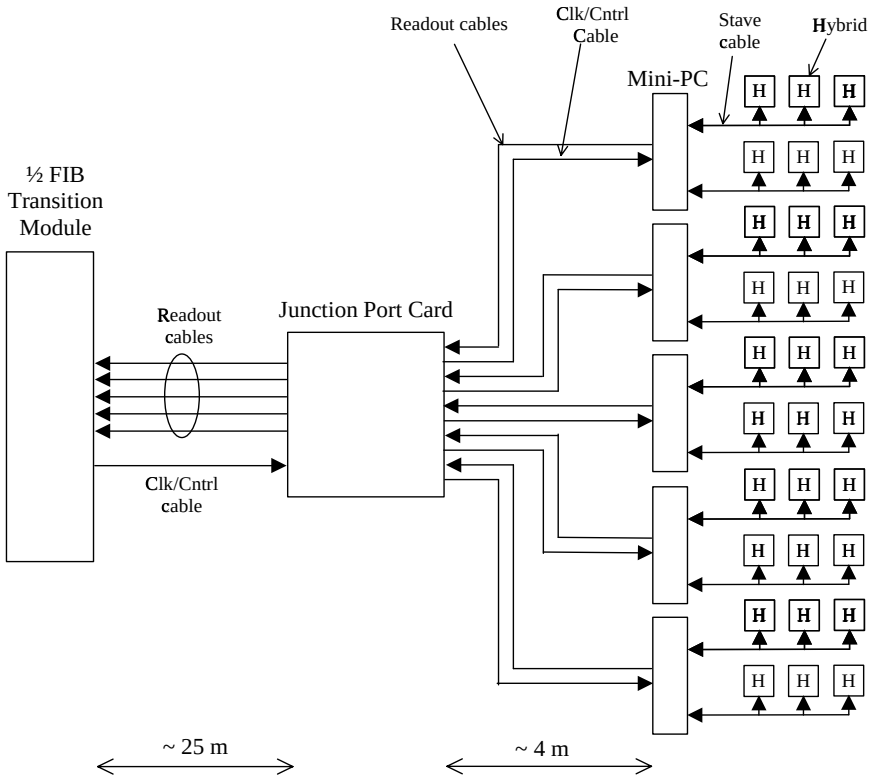

Figure 3.17: Block Diagram of the new components of the Run IIb DAQ (from Hybrids to Copper FTM's)

constraint on the total readout time for both. However, if many L1 triggers are rejected after 20 μsec, this will free up the L1 buffers making this constraint less important. Studies with Run IIa data have been used to estimate the allowed readout time for the Run IIb detector layout. The readout times for Run IIa ladders are added together such that they correspond sections that are roughly the same size as the proposed Run IIb staves. The studies are described in detail in reference [12]. They found that the coarser granularity of Run IIb design at low radius (particularly Layer 1) will not introduce significant deadtime in SVT.

3.5.3 Hybrids and Staves

This section describes the design of the SVXIIb readout hybrids and the stave electrical design. The design presented below assumes that each stave will contain one readout chain. Studies, with Run IIa data, of actual readout times and the execution time of the SVT trigger indicate that one readout chain per stave is sufficient.

The hybrids are circuit boards which service the SVX4 front end chips. They provide an interconnect to cables from the MPC and hold additional passive components which are required for the proper operation of the SVX4 chips. Key issues connected to the hybrids are material, reliability, and fabrication. If the hybrids are in the tracking volume, as they are in SVXIIa, they add to the passive scattering and conversion burden. As interconnects to the DAQ they must be reliable. Typically, a fabrication constrained to provide reliable, fully tested and characterized hybrid assemblies has been a major portion of the labor during the construction phase of past silicon trackers.

The hybrid requirements and philosophy for SVXIIb are discussed in the Run IIb Working Group report [1]. A guiding principle was to utilize as much of the Run IIa experience with L00, SVXIIa and ISL as possible. For example, for the Run IIb hybrids we will exploit the new fine pitch thick film etched technologies which worked very successfully on L00. We will also minimize the number of distinct hybrid designs in order to simplify and expedite the construction phase. In order to limit rework, a premium is placed on reducing the number of chips on a hybrid while maintaining an efficient readout configuration. The hybrid concept and design for Run IIb have been strongly influenced by the factors discussed in the working group report report. In addition it has taken into account later experience with the installation and commissioning of the Run IIa system and constraints imposed by a practical detector layout which meets the tracking performance goals for Run IIb.

Layer 0, the beam pipe layer, is similar to the Run IIa L00 design. The hybrids will be placed outside the tracking volume and connect to single sided axial sensors via fine pitch cables. In the new design all the Layer 0 detectors and hybrids will be identical. The detectors will be 256 strips wide and the hybrid will contain two SVX4 chips. As in L00, the hybrid substrate material will be Alumina since it is placed outside the tracking volume and cooling is not a critical constraint. The performance and yield of the L00 doublet hybrid were excellent thus we expect a similar result for the new project. The new L0 hybrid will require a transceiver chip on each hybrid since insufficient space will exist for nearby mini Port Cards. Considerable experience exists with operation of the transceiver chip on the hybrid from the ISL project. The total number of hybrids required for the beam pipe layer is 72.

Layers 1-5 are double sided stave structures in which the hybrids are glued to the silicon, as described in section 3.2.2. Built into a stave is an electrical bus structure to provide signals and current to the SVX4 chips. The hybrids will be considerably smaller than previous SVXIIa and ISL designs due to the use of the fine pitch hybrid technology developed for L00. The hybrid substrate material will be BeO. There will be 6 hybrids per stave, 3 on each side. Layers 1-5 all use 4 chip hybrids on both the ϕ and the stereo sides. A total of 1080 4-chip hybrids will be needed. Unlike SVXIIa, the hybrids will not contain "finger" structures between the chips to provide local AC bypass and biasing resistors. This simplification is due again to the use of fine pitch technology. The basic design of a 4-chip hybrid is shown in Figure 3.18.

A material estimate for the stave design is discussed in Section 3.7.

As indicated above, the hybrids will be serviced by an electrical bus structure running below the detectors. The electrical bus is a copper-kapton flex cable which is laminated to the carbon fiber surfaces of the stave. The single sided silicon sensors are glued on top of the cable.

Small gaps, $\approx$3 mm wide, between detectors allow wire bonds to be placed between the bus and the hybrids. This wire bonded interconnect eliminates the

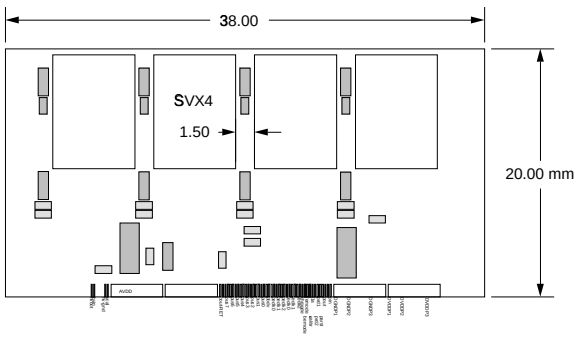

Figure 3.18: SVXIIb 4 chip hybrid used on Layers 1-5.

need for a separate cable or connector field on each hybrid and further reduces the hybrid area. The bus uses a differential transmission line structure and is shown in Figure 3.19. The traces are arranged in an edge coupled differential configuration. Lines are 75 microns wide with a 100 micron space. Each pair is separated by a 150 micron gap. The singled ended lines which provide slow control to the SVX4 chips use the same structure but are not paired. Power and ground are provided on wide traces to avoid excessive voltage drops and go individually to each hybrid. The impedance of the bus is determined by the trace geometry and kapton thickness between the bus and the carbon fiber below and the Aluminum shield above. Calculations have placed this at 85 ohms.

Tests are in progress with SVX3D chips to study shielding and power distribution in order to avoid electrical pickup from the bus structure. A thin (12 micron) layer of Aluminum for the electrical shield and a layer of Kapton to stand off the voltage on the back of the sensor has been shown to shield activity on the power and differential data lines. Some pickup can be seen due to activity on the slow control lines which are pulsed between operating modes of the SVX3 chip from 0 to 5V (CMOS) and this is still under study. The possibility also exists to run these lines differentially and install transceivers on the all the new hybrids. The situation can improve with additional shielding and with the lower voltage swings (0 to 2.5 V) in the SVX4 chip. A full understanding of these issues awaits the first full stave prototype with the new SVX4 chip.

The configuration and technology choices described above for hybrid and stave design and configuration are justified by the following considerations.

1. Material and temperature are most critical on the innermost layer. For this reason we chose to maintain the basic L00 design on the beam pipe layer with hybrids, and their heat load, outside the tracking volume.

2. Experience with the fine flex cables used on L00 for Run IIa was mixed. There are serious concerns about availability and cost for these parts in large quantities. In L00 these structures were found to be vulnerable to noise pickup although techniques for controlling this problem are largely known. Assembly of a complex structure using fine cables is awkward. For these reasons, a design which minimizes the use of fine line cables and applies them only where most appropriate was favored.

3. By placing hybrids on the silicon we can minimize dead space but this degrades the resolution in the covered regions. There is considerable power dissipation on the hybrids and this increases the cooling requirement on the silicon. For these reasons we restricted on-detector hybrids to the non-beam pipe layers.

4. The hybrids built for SVXIIa and ISL used a technology with a minimum 100 micron line and space width and 400 micron via pitch. For Run2a L00 we obtained a new technology which can accommodate 50 micron lines and spaces and 100 micron via pitch. With smaller vias and pitch we can reduce the area of the hybrid. In addition, the specific stave geometry allows us to combine trace and power/ground layers on the SVXIIb hybrids for Layers 1-5. This reduces the number of conductor layers from six to four. These space and material improvements mitigated concerns about mounting hybrids on the silicon for the non-beam pipe layers.

5. The manufacture and assembly/testing of the hybrids is a major construction burden. The SVXIIa, L00, and ISL had 13 distinct hybrid designs. For SVXIIb this has been reduced to 2 designs. We actually imposed a limit on the number of different hybrid designs on the layout configuration for the detector. This, in part, drove us to the particular stave based design adopted. With a reduced number of hybrid designs manufacturing is more efficient. Costs are reduced, particularly for the Layer 1-5 design.

For the hybrid and stave design to be viable the assembly and test process must be consistent with the schedule for Run IIb. We have considered this process and believe it can be organized to meet the required schedule. Below we elaborate on this plan.

1. The Layer 0 hybrid count is similar to L00 from

Run IIa. This is a known process and went rapidly without any particular difficulty. The entire project is <100 hybrids including spares and yield. Transceiver yield on hybrids for Run IIa ISL was nearly 100%.

2. The stave layers consist of a single four chip design. All the hybrids can be produced in one or two lots from the thick film vendor. Typical manufacturing time is 8-12 weeks.

3. Figure 3.20 indicates the steps involved in assembling and testing the stave layer hybrids. All operations except the stave lamination and final stave assembly are duplications of the Run IIa assembly process. While some new mechanical fixturing will be required, all the electrical test and burn-in hardware and software from Run IIa can be re-used.

4. The stave layer hybrids are attached to the stave bus by wire bonds. In the past, the flex cable or connector attachment process was time consuming and expensive. Elimination of this step represents a significant simplification.

5. Figure 3.20 indicates the rates needed from the component lines to produce one working stave per day during the construction cycle. Based upon Run IIa, this is reasonable and actually represents a lower production rate than that achieved in Run IIa.

3.5.4 Mini Port-card

The MPC will be mounted at the end of the stave and electrically connected to the end of the phi and z side stave buses with wire bonds. The MPC, as the hybrids, will be a fine pitch thick film circuit on a BeO substrate. All active circuitry will be on one side of the MPC. Each MPC will contain five transceiver chips, and by-passing and termination components. A pair of short external flex cables (pigtails) will connect the MPC to a longer cable set from the Junction Port Card. A wire bond pad field will enable connection to the phi side stave bus. An additional flex cable (the "wing") will be soldered to the MPC and will bend around to the back side of the stave. It will be glued to the Carbon Fiber core and will be bonded to the z side stave bus. Fabrication and assembly/test issues are similar to that of the hybrids. Approximately 200 MPC will be required to readout the Run IIb detector. Below we discuss the electrical design and expected performance of the MPC.

Figure 3.21 shows a block diagram of the MPC and its interconnection with the stave readout circuitry. Figure 3.22 shows the actual layout of the MPC com-

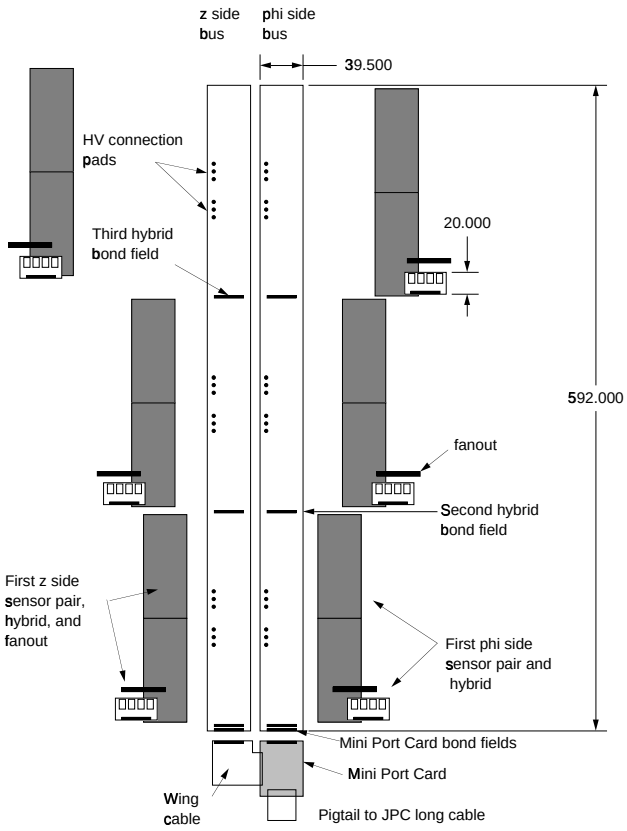

Figure 3.19: Stave bus stripline structure near the bonding region to a hybrid. Traces narrow for reasons of mechanical limitations and then widen between hybrids to maintain minimum voltage drop. HV lines are at extreme left.

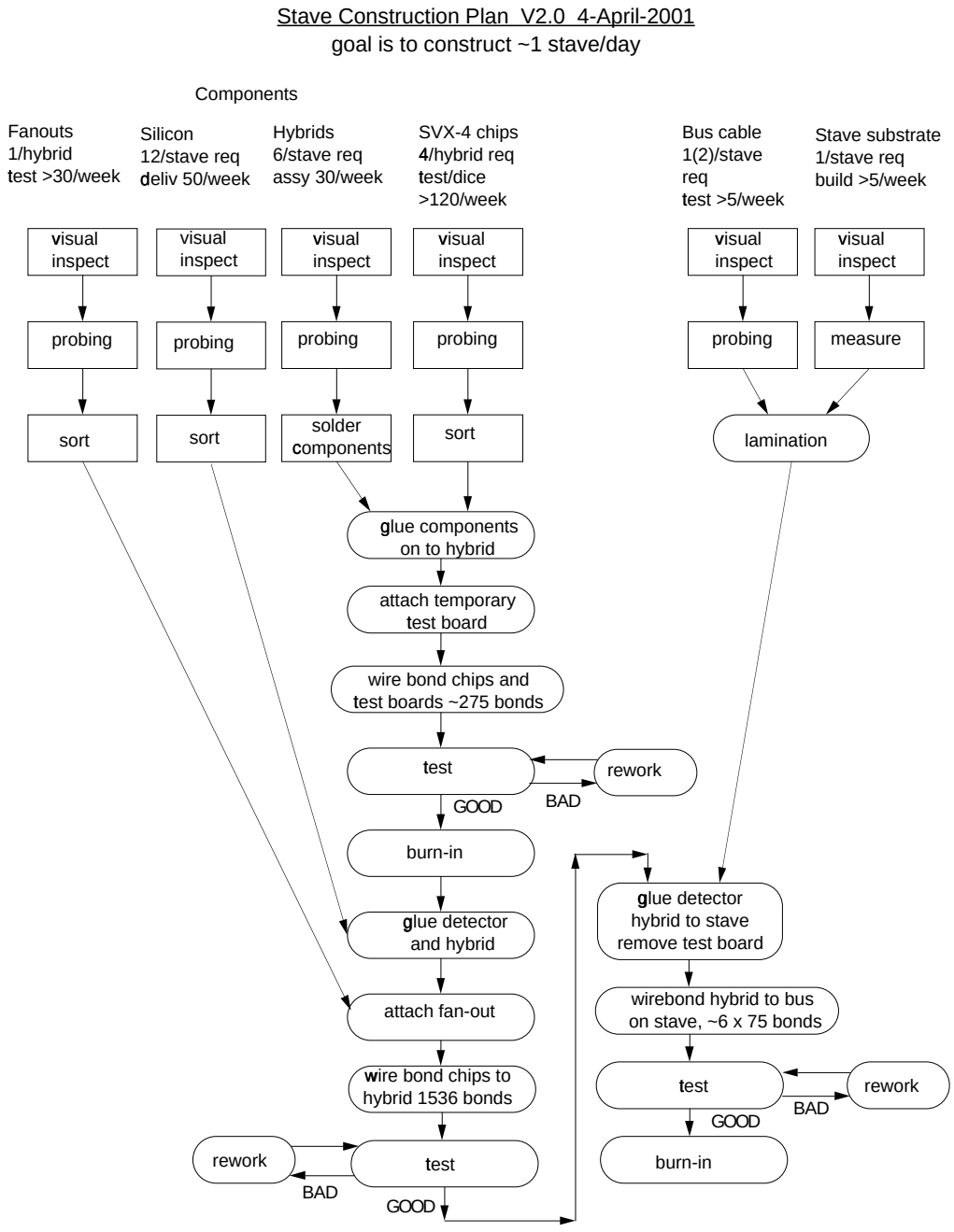

Figure 3.20: Construction and testing steps for stave hybrids

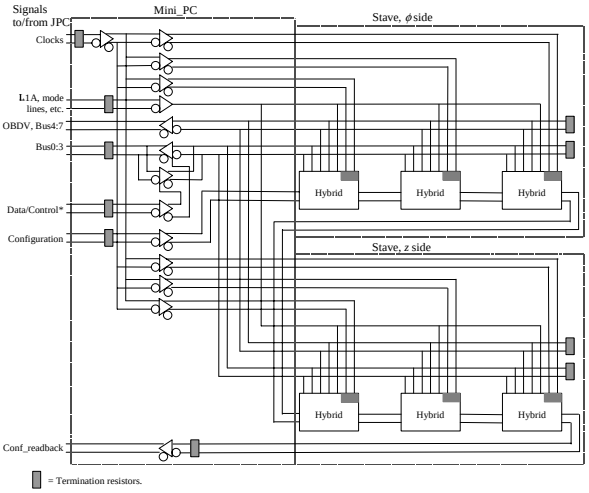

Figure 3.21: Block diagram of mini portcard and connections to hybrids on a stave

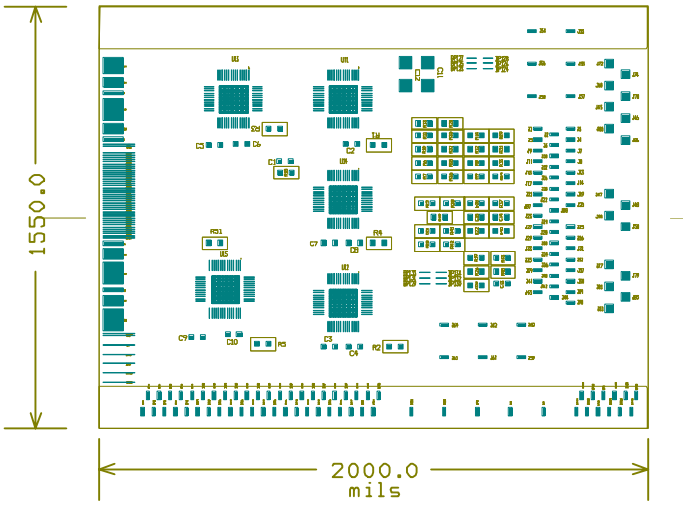

Figure 3.22: Layout of the MPC. Bond pads for the top stave bus cable are on the right. Solder pads for the wing cable are along the bottom. The solder pads on the left are for the external pigtail cables.

ponents and bond/solder pads. The MPC main functions are to buffer the signals between the hybrids and the JPC and to connect common signals and power supplies to the ϕ and z side of the stave cable.

All communication between the MPC and the JPC use LVDS since the JPC's will be relatively far ($\approx$4 m) from the staves. The clock lines (front-end and back-end) are regenerated on the Mini-PC and sent to each hybrid using dedicated drivers and dedicated differential lines. The clock termination is mounted directly on the hybrids. The SVX4 single ended control signals (CHMODE, L1A, etc.) are transformed from differential to single ended on the MPC. Most are bussed to all hybrids in parallel but those with critical timing (L1A and PRD2) are driven individually to the phi and z sides of the stave. The data lines are shared between the two stave cables and terminated on the last hybrid of each stave bus. Bus 0:3 lines are bi-directional and the differential drivers regenerate the data in both directions, from the JPC to the hybrids and vice-versa.

An important aspect of the interconnection of the MPC with the stave flex cables is the proper termination of the differential signals to avoid reflection on the lines. We have performed simulations to understand the termination schemes. A particularly critical signal is the differential Odd Byte Data Valid (OBDV). If a glitch occurs here, the DAQ system may store incorrect information. Figure 3.23 shows the result of such simulation with OBDV terminated as shown in the block diagram. The plot shows the two differential signals (OBDV and OBDV*) arriving to the OBDV differential input gate. The hybrid closer to the MPC is driving the OBDV. These simulations where done using Spice. The driver used was the Spice description model of the transceiver differential driver; the MPC, stave cables (top and bottom) and wing where simulated with a Spice lump transmission line; the wire bonds by 2 nH inductors and the chip inputs by 2 pF capacitors. Table 3.11 shows the characteristics of each transmission line of this chain. In the simulation, the stave busses on both the ϕ and z sides are 35 cm long. One can observe that, after the signals switch, there is voltage ringing but it is small enough to display a minimum differential voltage between OBDV and OBDV* of $\approx$350 mV, which insures that no glitch will happen. The ringing is produced by discontinuities on the transmission line caused by hybrids, wire bonds, capacitive load of the chips and impedance discontinuities from one type of transmission line to another (e.g., from stave cable to wing, etc.).

The MPC could use the Run IIa transceiver chips to generate the single ended 2.5V CMOS signals needed to control the SVX4 chips. Sufficient transceiver chips remain from the Run IIa project and are available to

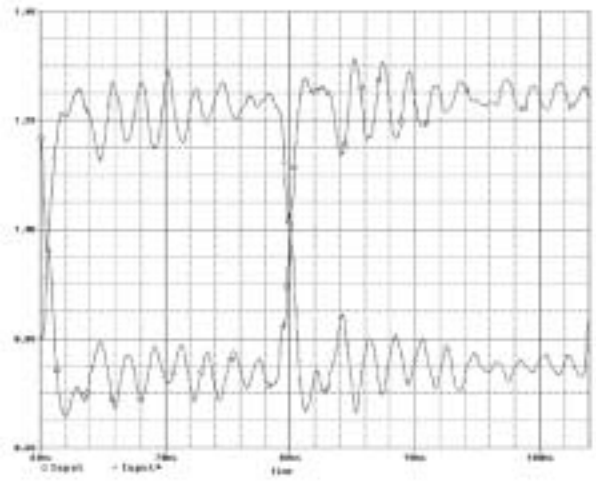

Figure 3.23: Differential Signals OBDV and OBDV*

	Hybrid	Wing	Bus	MPC
Differential Z(Ω)	68	83	85	70
Substrate ε	7	3.9	3.9	7
Ground Plane				
Top (μm)	-	-	75	-
Bottom (μm)	80	100	75	120
Traces				
Length (cm)	2.5	5	35.5	5
Width (μm)	50	75	75	75
Separation (μm)	50	100	100	75
Thickness (μm)	10	18	18	10

Table 3.11: Elements and configuration of the data chain simulation.

Capacitive Load	Rise Time	Fall Time
82pF	15.5ns	16.2ns
220pF	36.2ns	42.5ns

Table 3.12: Timing of Single Ended Transceiver Output with Capacitive Load

use in Run IIb. The transceiver chip was designed to operate with a 5.0V power supply. To use Run IIa chips, the non-inverting half of each differential output is converted by supplying 2.5V power to a dedicated driver current pin, and appropriately connecting ground or power to special pins that control the behavior of the differential outputs.

Table 3.12 shows how the rise and fall times (10-90%) of the single ended transceiver output varies with different CL when configured to convert a 5.0V input to a 2.5V output. This timing was measured using a transceiver irradiated with 18 Mrad (Co60 source). The capacitive load of all six hybrids, top and bottom stave cable, MPC and wing cable is estimated in 200 pF. The achieved speed for 220 pF is fast enough for most SVX4 single ended inputs but those, as pointed before, with critical timing (L1A and PRD2) are driven individually to the ϕ and z sides of the stave to reduce the capacitance to one half ($\approx$100 pF).

The radiation tolerance of the transceiver chips was studied by irradiating them upto a dose of 18 Mrad (Co60 source). Little degradation was seen in the signal quality for chips operated with 2.5 V output level, set to be compatible with the SVX4 chip. A second and more favorable possibility for the MPC is to use a new transceiver chip which can be designed on the same 0.25um technology of the SVX4 chip. The major advantages will be lower power dissipation and mostly the fact that a special 5V line for the transceiver chips would not be necessary. The latter results in a major savings in terms of power supplies channels and cables. At the time of writing a new transceiver chip has already been designed and submitted to MOSIS for verification with the plan of inserting it in the second svx4 chip submission. The transceiver chip occupies so little real estate in the silicon wafer that can be accomodated in the empty space left over by the svx4 chip reticule. Figures 3.24 and 3.25 show the results for 1 and 18 Mrad with 220 pF capacitive load. These studies are detailed in reference [11].

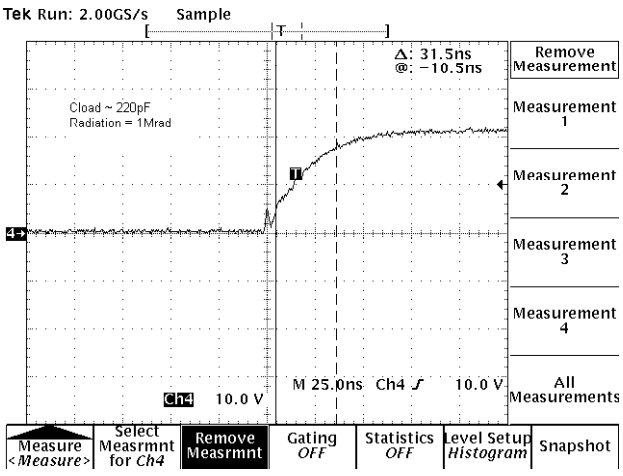

Figure 3.24: Risetime for 220pf load

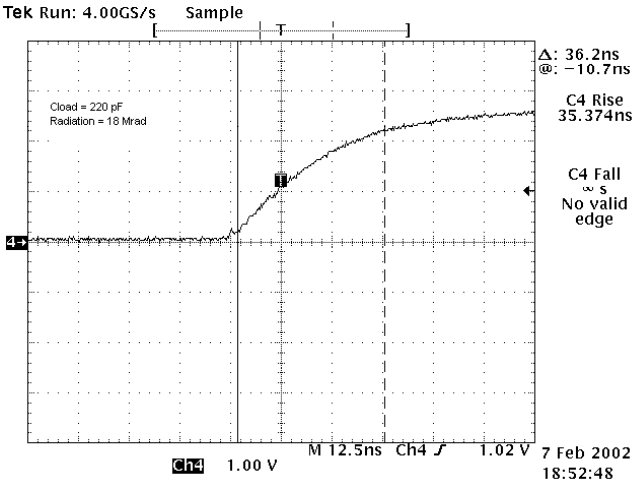

Figure 3.25: Risetime for 220 pF load and 18 Mrad dose.

3.5.5 Junction Port Cards (JPC)

The JPC will encompass the remaining functions of the Run IIa PC and Junction Card. On the JPC the read out data will be resynchronized to reduce the skew between different data lines and increase the data reliability. Voltage regulators will be needed for each readout chain and will produce some heat load. Each JPC will have 2 voltage regulators serving each MPC since voltages on both analog and digital power supplies will need control. Each JPC will connect to 5 MPC's, since there is one readout chain per MPC. As described in the introduction, the JPC will be located outside the tracking area, on the face of the central calorimeter. This is a low radiation area, with ample cooling and space available. As a result, the JPCs can use standard printed circuit board technology and off-the-shelf components in standard packages.

3.5.6 Cables

The MPC will be have two small low mass flex pigtails ≈12 cm long soldered to it. The pigtails will connect to low mass standard cables which traverse ≈ 70 cm the end of the ISL extension cylinder (the current location of the RunIIa junction cards). At this location, connections will be made to the ≈ 4m long cables which carry the data and control signals through the cable slots to the new JPCs on the COT repeater card ring. These cables will be a custom designed copper shielded cable with ≈24 pairs of 34 AWG wires and total diameter of ≈4.5 mm. Power and high voltage will use cables similar to the cables already employed in SVXIIa. In the Run IIa each port card corresponds to five readout chains, and the cables from each portcard occupy one slot. For Run IIb, each stave is a readout chain. Figure 3.26 shows the cables from 5 staves fit easily into one slot and thus the Run IIb detector will occupy the same number of slots as in Run IIa.

¿From the JPCs the cables go to the DAQ racks and power supplies which are mounted on the walls of the collision hall. These cables are similar to the cables used in SVXIIa and are commercially available.

3.5.7 FTM's and associated modules

The use of copper data cables instead of fibers from the MPC on out, necessitates a redesign of the Fiber Transition Module (FTM). We have performed several bit error rate tests with the appropriate LVDS

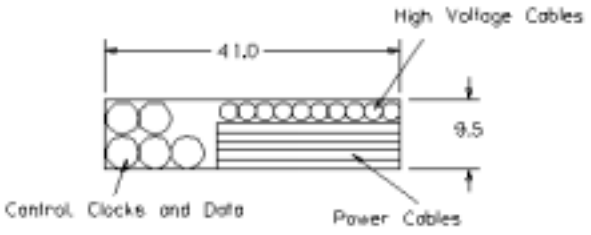

Figure 3.26: Cables from 5 staves fit easily into one of the COT slots.

drivers and receivers over 30 m of copper cables to test the reliability of such transmission. For example, LVDS drivers transmitting data at 53 MWords/sec over 30 m of copper ribbon cable have shown an acceptable bit error rate of better than 4.3×10^{-16}. This translates to one error every 3.8 hours if all SVXIIa ladders were transmitting data 100% of the time.

3.5.8 Power Supplies

The Run IIb power supply system will use the present infrastructure as much as possible to minimize costs and installation and testing time. In particular we will use the same scheme for interfacing the new power supplies with the CDF High Voltage control system (via the CAENET to VME interface board V288) allowing for the overall software infrastructure to remain the same (except for the low level specific CAEN instructions).

Power supply modules will necessarily be different from the Run IIa supplies for several reasons:

1. the SVX4 chips works with 2.5 V (not 5V);
2. all special voltages related to the optical transmission lines have been dropped;
3. the organization of the power distribution is based on *staves* and not on *wedges*;
4. it is desirable to use commercially available products rather than custom made ones.

Low voltage power should be provided separately to the analog section of the chip (AVDD), the digital section of the chip (DVDD), the MPC (transceiver chips), and the JPC. High Voltage will have a single polarity (positive) since we only have single sided detectors. Table 3.13 shows the different low and high voltage channels needed for the Run IIb silicon detector as compared to SVXIIa.

Power channels are grouped into power super-channels in order to provide power to a detector subsystem (for the SVXIIa super-channel would correspond to a ladder). A further combination of channels and super-channels capable of providing power to the part of the detector controlled by a single JPC (such a grouping for SVXIIa controls a wedge) is quite cumbersome to implement for this design (one JPC services 5 readout chains and we have 1 readout chain/stave). We are instead considering a scheme where JPCs are treated as separate channels and the natural grouping is implemented in software rather then in a physical module. Using this scheme we can count the number of channels and super-channels needed to power the system. Table 3.14 shows the counting in the model that a super-channel provides power to a single stave and consists of a single AVDD, DVDD, MPC and two Vbias (one for the axial and one for the stereo silicon detectors). As mentioned earlier in the section regarding the MPC, with the use of a new transceiver we can avoid providing the extra 5V line necessary to power the old transceivers in the MPC. The new transceiver will instead be powered by the DVDD line of the stave.

Table 3.15 compares the Run IIb approach of Table 3.14 with the present SVXIIa+ L00.

3.5.9 Failure Mode Analysis

The stave unit is highly integrated. This results in a significant reduction in mass, size, and readout and assembly complexity. The cost is increased vulnerability to single point failures. On each side of the stave there are three hybrids. All six share the output bus. In principle a failure on one can bring the entire stave down. This possibility is made significantly remote by various design and assembly features.

We currently are planning to use a special chip on each hybrid called the Priority Bypass Chip (PBC). This chip, when activated, causes the Priority and Initialization bits to bypass the hybrid. The chip is wired to both AV and DV. If DV is removed the chip is activated. Power is supplied individually to each hybrid on a stave. Thus we can activate this chip on a single hybrid if needed. The PBC would be used in a case where Priority became stuck in that particular

Run2b	Volt	I_{max}(A)	SVXIIa	Volt	I_{max}(A)
DVDD	2.5	0.15/chip	DVDD	5.0	0.15/chip
AVDD	2.5	0.25/chip	AVDD	5.0	0.15/chip
TRX	5	1.0/MPC	+5VDOIM	5.0	2.8/PC
JPC	5	4.0/JPC	+2VDOIM	2.5	-1.7/PC
			DTERM	3.5	±0.15/PC
Vbias	600	0.01/half stave	Vbias	±250	0.005/Layer

Table 3.13: Power need for the present silicon system as compared to the SVXII. Currents are estimated using the minimal approach from Table 3.14.

Layer	R/O Chains	JPC	LV	HV
5	60	12	192	120
4	48	10	154	96
3	36	8	116	72
2	24	6	78	48
1	12	4	48	24
0	72	16	232	72
TOTAL (both sides)	252	56	820	432

Table 3.14: Number of R/O chains, JPCs and separate Low and High voltage channels needed. Note that the R/O chains are split evenly between the East and West sides of the detector and there are at most 5 R/O chains per JPC on each side. L0 has one R/O chain/module. For layers 1-5 the number of LV channels assumes 3/stave(AVDD, DVDD and MPC) + 1/JPC. Two HV channels per stave are assumed. For Layer 0 for LV we assume 3/module (AVDD, DVDD and one for the transceiver) + 1/JPC, and for HV we assume 1/module.

Layer	R/O Chains run2b	R/O Chains svx2+l00	LV run2b	HV run2b	LV svx2+l00	HV svx2+l00
5	60	72	192	120	144	72
4	48	72	154	96	144	72
3	36	72	116	72	144	72
2	24	72	78	48	144	72
1	12	72	48	24	144	72
0	72	48	232	72	96	60
Port Card					216	
TOTAL	252	408	820	432	1032	420

Table 3.15: Number of separate Low and High voltage channels for Run IIb as compared to SVXIIa + L00

hybrid. It would also be used in a case where a hybrid or chip took control of the data bus but would release it if DV was removed.

Failure modes effecting the consumption of analog current are potentially serious since AV cannot be turned off with DV on, and if both are off the PBC won't work. In this case we lose that hybrid and all after it on the stave. Failure modes effecting the consumption of digital current should be isolated to one hybrid if the PBC is used to bypass it. Failures of a single wirebond on a data or control line can result in either a loss of data from a single chip or the entire hybrid. In some cases the chip or hybrid could be left stuck in a state which compromises the function of the bus. In this case the PBC could be used to recover the rest of the stave. If we needed to bypass priority and the PBC failed then we could lose the stave after the offending position. If the PBC failed in such a way that it shunted Priority against our desire, then we would lose the hybrid.

On power and ground pads from the stave bus to the hybrid, multiple wire bonds will be used to reduce the danger of bond failure. On the data and control lines, the bond pads are narrow and multiple bonds may not be possible. This will however be explored with the stave prototyping program. Whenever possible, chip to hybrid bonds will be doubled up as well. Bonds from the mini-PC to the bus are critical since a loss there could compromise the entire stave.

Problems with the PBC or excessive AV current could be mitigated if the the PBC was served by a dedicated power line common to all hybrids. This will be explored in the prototyping program. Bonds to the stave and from chip to hybrid will be encapsulated with room temperature cure Sylgard 186. This material has been used extensively in the Layer00 project with excellent results. All component connections on the hybrid will use solder rather than conducting epoxy to avoid the possibility of cracks in the bond.

3.5.10 Summary

A design for the readout of the Run IIb detector has been presented. The various components have been detailed and are fairly straight forward. This system moves material further out of the tracking volume and makes maximal use of SVXIIa components and experience. The DAQ will be the same from the FTM's on up the readout chain. Although Run IIb has more channels, abandoning the wedge design has allowed us to optimize the readout chain distribution and thus the total number of DAQ chains will be smaller than in Run IIa.

3.6 SVX4 Chip

The silicon signals will be integrated, digitized, and read-out locally by a custom integrated circuit (chip) designated SVX4. The SVX4 chip is a functional replacement of the SVX3 chip used in the Run IIa silicon detectors with some important differences.

1. A lower noise and faster rise-time amplifier, which allows for larger detector capacitances.
2. Lower operating voltage (2.5V instead of 5V).
3. Enhanced radiation tolerance.

The SVX4 development work began in 2000 after it was realized that the SVX3 chip had several limitations that made it a poor candidate for instrumenting a Run IIb upgrade, and that such an upgrade would only be possible if a viable readout chip was available. The main disadvantages of the SVX3 readout chip are as follows:

1. Radiation tolerance is not adequate for Run IIb inner layers, and noise increases significantly with radiation for outer layers.
2. Amplifier noise and rise-time are unfavorable for large detector capacitance values.
3. Manufacturer (Honeywell) increased production costs to a prohibitive level.
4. Severe yield problems were encountered during Run IIa construction that were not well understood and could not be prevented for a future run.

The SVX4 chip design is complete and an engineering run submission is in progress. Full prototypes will be available in summer 2002. The design is the work of a collaboration of engineers from LBNL, Fermilab, and the University of Padova. The design targeted the 0.25μm feature size bulk CMOS process of the Taiwan Semiconductor Manufacturing Company (TSMC). This is a commercial process that is not advertised as radiation hard, but the thin gate oxide used in deep sub-micron processes is inherently

"immune" to radiation damage, and by using special layout techniques developed by the RD-49 collaboration for LHC experiments, can yield devices with very high radiation tolerance. However, while the SVX4 chip is functionally a replacement for SVX3, many sub-circuits required significant redesign to adapt to the new technology. The amount of design work that has been done runs the full spectrum from the ADC, where the schematics are identical in SVX3 and SVX4, to the data memory ("FIFO"), where a completely new circuit with a radically different architecture has been implemented for SVX4. In the latter case the deep sub-micron technology is so much faster than the technology used for SVX3 that the FIFO could be built out of standard circuit elements (available as a library developed by RD-49) and a layout automatically generated using commercial software. This is in contrast to SVX3 where the FIFO was fully custom made and used innovative circuit ideas and dynamic logic to be able to perform at the required speed.

Because the SVX4 chip required significant redesign, a list of specifications was produced early on to provide a frame for the engineers to work in. This list was generated jointly by CDF and D0, as D0 intends to also use the SVX4 chip in their Run IIb upgrade. The SVX4 design specifications are reproduced in Tables 3.16, 3.17, 3.18, and 3.19.

¿From an operational standpoint the most significant impact of the move to deep sub-micron technology is the lower operating voltage, 2.5V instead of 5V. In order to use the SVX4 chip in a system that was designed for 5V electronics it will be necessary to shift logic levels of many signals. Fortunately the radiation tolerant "Transceiver Chip" that was developed for the present detector can be used as a level shifter although it was not designed as such. A less obvious consequence of the lower voltage is that the tolerance for voltage drops in power supply lines is greatly reduced, which has implications for power distribution and voltage regulation. Finally, the maximum achievable dynamic range of the front end amplifier is necessarily lower than in a 5V process, but this is not an issue because there is significant headroom in this parameter.

As previously mentioned, significant design work was involved in generating the SVX4 chip even though it is roughly a functional replacement for SVX3. This is because the deep sub-micron process is sufficiently different from the process used for SVX3 that simply copying over the SVX3 schematics does not work in general (although it does work very well for some circuit elements). In particular, the lower voltage has implications for many circuits, but also the special design rules needed for radiation tolerance have an appreciable impact. A significant amount of simulation and design verification was performed by the engineering team. No features were left out of the engineering submission, in hope that it may work as final prototype. The schedule does however allow for one additional iteration of the design. Confidence in the viability of the first engineering submission is supported by by two main factors. Nevertheless, (1) The basic architecture of the SVX4 chip is copied from SVX3 and the desired relation between inputs and outputs is exactly known. (2) Because a standard commercial process is being used, the accuracy of simulation tools is vastly superior to what was available during SVX3 development. Even for detailed characteristics of analog circuits, measurements and simulation are seen to agree at the 5% level. This has been verified with a brief test chip program.

Two sub-circuit test chips have been fabricated as part of the SVX4 development. A preamp only chip was received from the MOSIS prototyping service in February 2001, and a preamp plus pipeline and logic controller chip was received in July 2001. The former was submitted at a very early stage of the design work, and was used throughout the design process to verify simulation results and later on to check the radiation tolerance of the process. This chip was irradiated in a Co^{60} source up to a total does of 40 MRad. No measurable difference was seen in the performance (noise, risetime, etc.). Transistor thresholds did shift measurably in good agreement with prior data from the RD-49 collaboration (even though they are from a different deep sub-micron manufacturer). The second test chip has also been irradiated up to 16 MRad and no performance degradation was seen at the 5% level. Bench measurements of this chip demonstrate that all front end circuits are fully functional and meet design requirements. The noise at the pipeline output using double correlated sampling is 30% less than for SVX3D, which meets the design specification. Beyond that, this second test chip was very useful in understanding some process parameters. Through this chip it was discovered that the foundry would default to a high resistivity substrate due to certain design elements in the SVX4 chip unless specifically instructed not to (the intent for SVX4 is to use a low resistiv-

A.	General:	
1.	Input bonding pad pitch:	48μm
2.	Overall Width:	6.250mm active area. Dicing streets as close as allowed by design rules.
3.	Overall length:	$<$ 11.925mm
4.	Supply voltages:	2.25-2.75V analog, 2.25-2.75V digital.
5.	Versions:	A version is the basic "conservative" version. B version adds on-chip bypassing and front to back combined power routing.
6.	Bond pad layout:	Both version have same bond pad layout with some pads used only by CDF and others used only by D0.
7.	Bond pads:	Except Front End inputs, no wirebond pad is to be smaller than 150 $\times$ 150μm (cover layer opening). Probe pads not meant for wirebonding are exempt.
8.	Maximum Supply Voltage:	3.5V
B.	Preamp:	
1.	Input pulse polarity:	Positive.
2.	Gain (feedback capacitor):	3mV/fC.
3.	Gain uniformity (ch-to-ch):	5% or better.
4.	External load capacitance:	10pF to 50pF.
5.	Risetime 0-90%:	adjustable in a range that includes 60-100ns for any allowed load.
6.	Risetime adjustment:	4 bits minimum.
7.	Noise (ENC):	2000e^- or less for a 40pF load using double correlated sampling with 100ns integration.
8.	DC open loop gain:	$>$2500 ($>$95% charge collection from 40pF).
9.	Linearity:	Linear response for pulses up to 20fC, non-linearity $<$0.25mV at output.
10.	Dynamic range:	$>$200fC.
11.	Reset + settling time:	$<$ 1μs for any initial condition.
12.	Reset offset voltage:	Internally set to a value TBD by designers, with external override capability.
13.	Input protection diodes:	2μA DC capability to either rail. Current must not go to substrate.
14.	Calibration injection:	40fF internal cap switched to input.
15.	Calibration charge control:	1 external analog reference voltage (other voltage is AVDD, not ground).
16.	Input disable switch:	2 Config. Register bits. N.1 disables control of reset switch for channel with calibration mask bit set. N.2 determines whether reset switch is always closed or always open for disabled channels.
17.	Input Device Current:	Adjustable with configuration bits as in SVX3 but with wider range (factor of 2).
18.	Bypass capacitors:	Performance in SVX-II mode to be maintained with no external bypass capacitors closer than 10mm.

Table 3.16: SVX4 Chip specifications part 1 of 4.

C.	Pipeline:	
1.	Input Pulse polarity:	Negative.
2.	Voltage gain:	3 to 5 (in that range, fixed).
3.	Gain uniformity:	5% channel to channel.
4.	Risetime, 0-90%:	10ns to 40ns (in that range, fixed).
5.	Noise (ENC at preamp input)	$< 500e^-$.
6.	Linearity:	linear response up to 20fC at preamp input.
7.	Dynamic Range:	To Be Confirmed: >40fC at preamp input.
8.	Reset Time:	<20ns for any allowed initial condition.
9.	Pedestal uniformity:	$< 500e^-$ at preamp input channel to channel, $< 1000e^-$ at preamp input cell to cell.
10.	Bias:	Internally set with override bonding pad.
D.	ADC:	
1.	Type:	Wilkinson with real time pedestal subtraction.
2.	Voltage Ramp:	Rate adjustable with external resistor.
3.	Ramp rate "trim" bits:	3 Bits, adding binary weighted capacitors to op-amp feedback. Largest capacitor is 4x the fixed feedback capacitor. These capacitors provide a range adjustment- no fine adjustment.
4.	Ramp Linearity:	0.25% for rates between 0.1 and 1 V/μs.
5.	Ramp dynamic range:	1V.
6.	Ramp pedestal:	Same as in SVX3.
7.	Counter:	8-bit Gray code, 106MHz rate.
8.	Differential nonlinearity:	<0.5 LSB.
9.	Bias:	Internally set with override bonding pad.
E.	Data output drivers:	
1.	Type:	Complementary with "resistor current sources".
2.	Current source range:	2.5mA to 17.5mA in 2.5mA steps (3 bit adjust).
3.	Rise and fall times:	>2ns and <4ns with nominal load.
4.	Common mode:	VDD/2 nominal with T termination.
5:	Load capability:	70Ω and 20pF.
7.	Tri-state:	Outputs tristated in initialize (except if SR copy pad is bonded- see H7) and digitize modes.
8.	Single ended use:	No additional requirements.
9.	Bidirectional:	All Bus pads will be bidirectional. Only some will be used of input as well as output by CDF, but all of them will be I/O for D0.
10.	Output data skew:	>3ns between OBDV and any bus line and between any two bus lines.

Table 3.17: SVX4 Chip specifications part 2 of 4.

F.	TN-BN Pins:	
1.	Functions	The multiplexed functions of the SVX3 TN/BN pads will be separated in SVX4 to TN/BN Priority in/out dedicated sets of pads.
2.	Type, BN/TN:	"Open collector" I/O with internal pull-up.
3.	Type, Priority in:	Differential receiver (2 bond pads) same as clock receivers, with added high Z common mode reference voltage (center tap of large R between VDD and
4.	Type, Priority out:	Differential driver (2 bond pads) same as data bus outputs.
5.	BN/TN Internal pull-up:	$> 500\Omega$.
6.	BN/TN Pull-down current:	>10mA.
7.	BN/TN Modes:	only active in digitize mode.
8.	Priority in/out Modes:	Configuration register input/output during initialize mode. Priority passing during readout mode. Priority out high during digitize mode.
9.	Bonding pads:	This increases the number of bonding pads per chip by 4 (2 next to TN and 2 next to BN).
G.	Configuration Register:	
1.	Type:	Bit serial shift register.
2.	Cell type:	SEU tolerant shadow register.
3.	Shadow register:	Keep as in SVX3 for SEU tolerance.
4.	Clock:	Register advanced with FE clock in initialize mode.
5.	Length:	As needed.
6.	Preset:	no preset.
7.	layout rule:	Do not place configuration register cells within 75μm of a wirebond pad (they can be destroyed by missed wirebonds).
8.	Bit order:	LSB loads first on all fields.
9.	Bit Assignment:	Numbers are for illustration. Designers may add bias adjust or other system bits as needed:
	0-127:	Calibration Mask
	28:	Cal-inject signal polarity
	29:	Input disable
	30:	Disable mode (reset always on or off)
	140-144:	Bandwidth bits (left room for 5)
	145-147:	Input transistor current
	148-153:	Pipeline depth
	154:	Pipeline readout order
	155-161:	Chip ID
	162:	Real time pedestal subtraction Enable
	163:	Last channel latch
	164:	Channel 63 latch
	165:	Read all
	166:	Read Neighbors
	167-170:	Ramp pedestal
	171:	Ramp direction
	172:	Comparator polarity
	173-175:	Ramp range selection
	176-183:	Sparsification threshold
	184-191:	Counter Modulo
	192:	First chip flag (see H.9)
	193:	Last chip flag (see H.9)
	192-194:	Output driver resistor select

Table 3.18: SVX4 Chip specifications part 3 of 4.

H.	Control Functions:	(*) Denotes desirable features but not strictly required.
1.	Signal Functions:	All control signals same function as SVX3 except as noted here.
2.	Ramp and Counter Reset:	Remove Counter Reset as an independent signal. In normal mode Counter Reset is to be tied to Ramp Reset. In Dynamic Pedestal Subtraction mode Counter Reset is internally generated as in SVX3.
3.	Preamp Reset & Fe Clock:	Preamp Reset should always function independently of FE Clock state. (In SVX3 Preamp Reset can only go high while FE Clock is high).
4.	Last channel SR bit:	on=always latch chan. 127 (same "last chip flag" in SVX3).
5.	Chan. 63 latch SR bit:(*)	on=always latch chan. 63 (doubles read out speed).
6.	extra L1A:	Additional L1A pulses (beyond 4) should be ignored by the pipeline logic.
7.	OBDV (data valid) control (*):	OBDV must be driven by 1 chip per daisy chain at all times to prevent data transmission errors. This can be accomplished in SVX4 with 2 configuration register bits: First Chip (FC) and Last Chip (Different from item 5). OBDV control is given by this logic table

Pri. In	Pri. Out	FC	LC	OBDV
H	H	L	L	disabled
H	L	L	L	disabled
L	H	L	L	ENABLED
L	L	L	L	disabled*
X	H	H	L	ENABLED
X	L	H	L	disabled*
H	X	L	H	disabled
L	X	L	H	ENABLED

		* OBDV is to be disabled one BE CLOCK cycle after Pri. Out is lowered (same as in SVX3). [In the present CDF silicon system it was necessary to add logic to the port cards to implement this function, because the SVX3 does not have the FC and LC bits.]
8.	D0 Mode pad:	A special bond pad, if bonded will set the chip in D0 mode. This will multiplex I/O signals onto all Buslines and gate off the Pipeline Clock during digitize and readout operations.
9.	Test outputs:	Buffered preamp and pipeline outputs for one channel, Comparator output for 1 channel, Ramp probe point, RTPS comparator buffered input and output- all as in SVX3. Additional probe points as needed to fully test performance.

Table 3.19: SVX4 Chip specifications part 4 of 4.

ity substrate with an epitaxial layer just as was done for SVX3). A deficiency in the design rule verification that relates to the yield of precision capacitors offered in this technology was uncovered and corrected.

Presently submission of the chip is expected March 25th and wafers should be in hand for testing by late May. Figure 3.27 shows the footprint of the SVX4 chip (internal bonding pads are not shown). The engineering run will contain two versions of the SVX4 chip: SVX4A and SVX4B. The main difference between them will be the power distribution. In SVX4B new concepts will be tested using on chip capacitance to combine power supplies, thereby reducing the number of external connections and components required. Details of power distribution mainly affect performance in dead-timeless operation, which is a system issue difficult to understand with simulations. The features explored with SVX4B go beyond simply building an SVX3 replacement and were originally introduced to address requirements of the D0 collaboration, which will not operate the chip in dead-timeless mode but may have tighter constraints that CDF on available space for components and external connections. Which chip version is more suitable for CDF (A or B) will be determined from bench tests of the engineering prototypes. If it turns out that both CDF and D0 can use the same chip version, a joint production run of SVX4 would be possible. This would save some fabrication costs, but more importantly would reduce the total production testing effort.

3.7 Material

An important design goal of the Run IIb detectors was minimization of material in the tracking volume. This is particularly important in the innermost layers where multiple scattering degrades impact parameter resolution. Material at larger radii can also degrade pattern recognition performance, generate secondaries, and reduce electron identification efficiency.

The material for the Run IIb detector is estimated based on the layout presented in section 3.2. Figure 3.28 shows a schematic model of the materials in a stave. The dimensions are not to scale. The total material in a stave, averaged over the stave area, is $\sim 1.8\% X_0$.

In Run IIa, the SVXII readout hybrids are mounted in the active volume to minimize acceptance loss due to gaps, and the portcards are mounted in the tracking volume to minimize the distance between the readout hybrids and portcards. The data from the SVX3D chips are converted to optical signals on the portcard. While the fibers carrying those signals out of the detector volume are low mass as expected, their power consumption is substantial so that their cooling and power cables introduce substantial mass.

For the innermost layer, minimizing material was critical, so kapton signal cables are used to locate the readout hybrids out of the tracking region. This was also required by space constraints in Run IIa. Furthermore, L00 used long kapton bus cables to carry the data from the readout hybrids to portcards which were placed at large radius and large $|z|$, outside the tracking region.

The use of single-sided silicon sensors in Run IIb doubles the contribution of silicon to the material budget since a separate sensor is used for the axial and stereo measurements. But, as can be seen in Figure 3.29, silicon accounts for only a small fraction of the material budget in the Run IIa design. There are several ways in which the Run IIb design attempts to minimize material. The innermost layer uses kapton signal cables, like Layer-00, to keep the readout electronics out of the tracking volume. This keeps the material low for the critical inner layer. The use of a universal stave for the outer layers introduces new material from the carbon fiber support structure, the direct silicon cooling which is needed for radiation hardness, and the bus cable. But, the bus cable allows the removal of the portcard and power cable material since the mini-portcard will now be mounted at the end of the staves. The use of an LVDS copper data bus instead of optical readout does not increase the material budget because the lower power and cooling requirements more than compensate for the thin copper traces in the data bus. Finally, the new readout hybrids are smaller and lower mass than in Run IIa because of the compactness of the stave design and use of new printing technologies.

The material seen by a track is dependent on z (e.g., when a track goes through a hybrid region it sees more mass than when it misses the hybrids.) Figure 3.29 shows a comparison of the Run IIa and Run IIb design for 90^o tracks as a function of z. One can see that the material budget in the Run IIa design is large. The dominant material effects arise from readout hybrids, portcards, and power cables. In Figure 3.29 for z< 1cm the Run IIa material is only silicon. From 1-3cm it is Si and portcard cables. From 3-10cm RunIIa has silicon, portcard cables and portcards; from 10-20cm

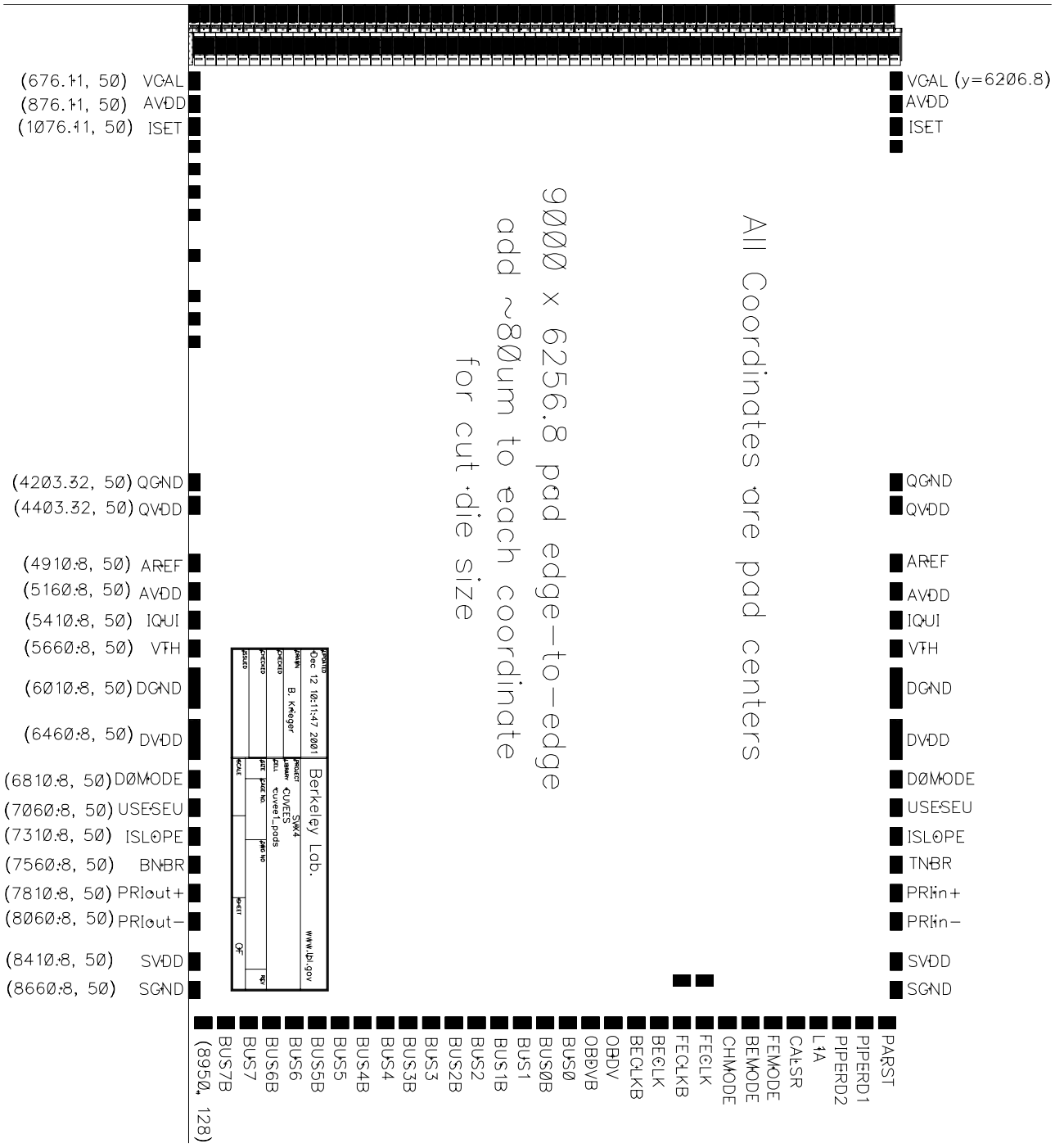

Figure 3.27: SVX4 chip pad frame specifications.

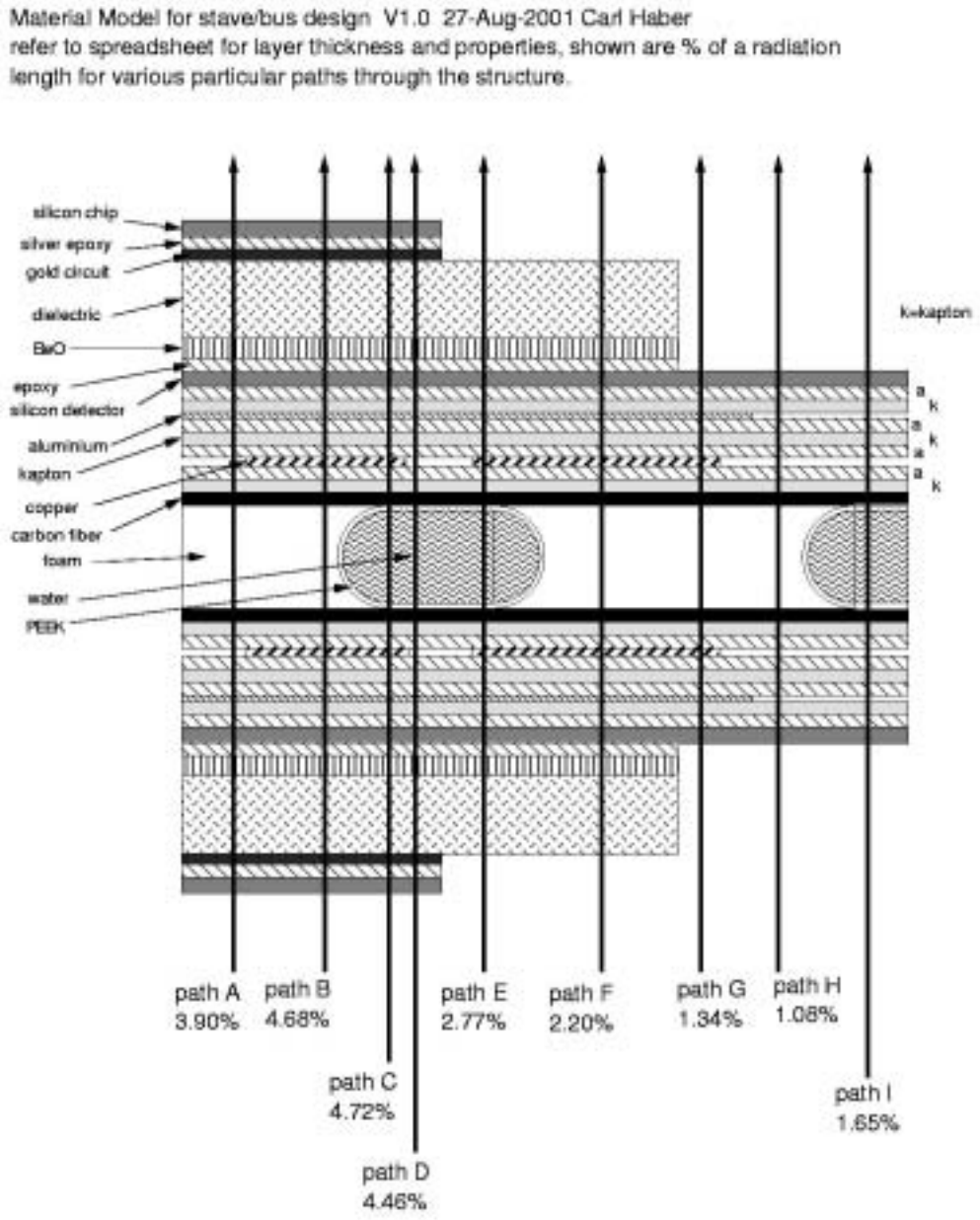

Figure 3.28: Material model for Run IIb stave design.

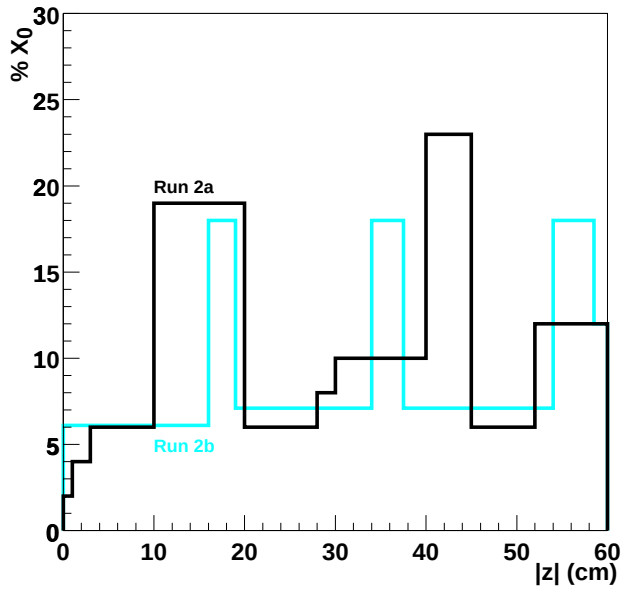

Figure 3.29: The average material of the Run IIa and Run IIb silicon detector designs is compared for normal incidence trajectories as a function of position along the beam line ($|z|$). The black curve is Run IIa. The light curve is Run IIb.

it is silicon, hybrids, portcards, and portcard cables. At larger z the pattern of silicon, hybrids and portcards repeats and the portcard cables pile up. The contribution in the Run IIa design from power cables is $\sim 4\% X_0$ from $3 < |z| < 28$ cm. It rises to $\sim 8\% X_0$ beyond that. The contributions from the readout hybrids ($\sim 13\%$) can be seen for $10 < |z| < 20$ cm and $40 < |z| < 45$ cm.

The expected material contributions in the Run IIb design shown in Figure 3.29 are: $\sim 6\% X_0$ for $|z| <$ 16 cm from silicon, carbon fiber support structure, and cooling; $\sim 18\% X_0$ due to the addition of readout hybrids in the regions at 16, 34, and 54 cm; and $\sim 7\% X_0$ for the remaining regions due to the bus cable beginning at the location of the first hybrid.

3.8 Descoping

The Lab has asked us to present descoping options as part of the technical design of the Run IIb silicon detectors. There are a number of choices that should be made during the project once it is clear how the schedules are proceeding. A dramatic candidate for descoping the project is to drop the outer layer. This would reduce the number of staves by 33%, but would result in a weaker detector. Studies using the Run2a simulation package have shown that this would have a negative impact on the b-tagging efficiency and thus would reduce the Higgs search capabilities of the detector. We prefer to consider a staged approach to descoping. The design of the outer layers is such that the staves are interchangible from layer to layer. If it becomes clear late in the project that the installation schedule will not be met, it is possible to simply rearrange and/or omit staves. This could result in incomplete layers, but would be have a smaller negative impact than dropping the entire outer layer.

3.9 Summary

We have presented a design which is based in great measure on the experiences with the previous CDF silicon detectors and on the R&D in progress for the LHC detectors. We have simplified the mechanical design and minimized the expected construction time by utilizing one stave design for the majority of the layers. The $r - \phi$ tracking capabilities should match or exceed that of the Run IIa detector and the the design should be able to easily withstand the expected radiation dose from Run IIb. We feel that this Run IIb detector can be built in the alloted time and will be sufficiently powerful to fully exploit the physics opportunities presented in Run IIb.

Bibliography

[1] T. Affolder et al, Run IIB Silicon Working Group Report, CDFNOTE:5425. Submitted to PAC in Oct. 2000.

[2] Charge from PAC.

[3] The CDF Collaboration, Run IIA Technical Design Report, Preprint FERMILAB-Pub-96/390-E

[4] N. Demaria et al, NEW RESULTS ON SILICON MICROSTRIP DETECTORS OF CMS TRACKER, Nucl.Instrum.Meth.A447:142-150,2000

[5] P. Azzi at al, Results on the SGS-Thompson Low Resistivity Silicon Detectors for L00, CDF/DOC/CDF/PUBLIC/5301.

[6] G. Bolla et al, THE CDF SVX II UPGRADE SILICON DETECTOR: SILICON SENSORS PERFORMANCES, Nucl.Instrum.Meth.A409:112-116,1998

[7] G. Bolla et al, SILICON MICROSTRIP DETECTORS ON 6-INCH TECHNOLOGY, Nucl.Instrum.Meth.A435:51-57,1999

[8] CDF Collaboration, Physics Performance of the CDFII Detector with an inner silicon layer and a Time of Flight (update of Fermilab proposal P-909), CDFNOTE 5264; March 2000.

[9] KEYCOM Co., 3-40-2 Minami-Otsuka, Toshima-ku TOKYO, Japan 170-0005.

[10] Andresen, J., et.al., "The Port Card for the Silicon Vertex Detector upgrade of the Collider Detector at Fermilab," IEEE Trans. Nuclear Science, Vol. 48, pp. 504-508, June 2001

[11] Turqueti, M., Weber, M., Zimmermann, S. "C0-60 Irradiation Tests Performed for the Ten Bits Differential Transceiver (Version B)," CD/ESE/Fermilab internal Document, Feb. 2002.

[12] D. Stuart "Silicon Readout Time and Event Size with Projections for Run IIb" CDFNOTE 5887, March 2002.

Chapter 4

Silicon Detector Design

4.1 Detector Layout

For Run IIb CDF plans to replace the SVXII and L00 detectors while retaining the ISL detector. The details of the mechanical design are presented in the previous chapter. As part of an integrated tracking system, the SVXIIb detector must provide robust tracking in the high luminosity environment of Run IIb. The similarities and differences with the Run IIa design are presented below.

- Similarities
  - A low mass, high precision, beam pipe layer with axial strips only.
  - Longitudinal segmentation of 6 readout modules.
  - Operation with the displaced vertex trigger.
- Differences
  - More uniform radial distribution of layers and no electronics or cooling between the outer layer of SVX and ISL
  - Use of single-sided sensors everywhere. Double-sided layers are made up of two layers of silicon with a few millimeters of radial separation.
  - A single structure is used for the outer 5 layers and the number of staves/layer increases with radius, rather than a wedge design where the size of the sensors in a wedge grows with radius.
  - Use of an intermediate strip everywhere to improve hit resolution while also keeping the channel count as low as possible.
  - Three or four small-angle stereo (SAS) layers to improve the association with axial tracks and the overall robustness of the system at high luminosity.
  - A larger radius for the beam pipe layer.
  - A double-axial layer just outside the beampipe layer.
  - The outermost layer has the option of being a double axial layer, as described in Chapter 3, or made of axial and small-angle stereo sensors as Layers 2-4. The small-angle stereo option would be chosen if the ISL is not fully repaired or if further studies of the performance at high luminosities indicate the additional stereo measurement is more desirable. Retaining this option with Layer 5 has little impact on the cost and schedule of the project and allows us to react to the outcome of the ISL repairs.

The use of intermediate strips in the designs of all sensors is made possible by the fact that we anticipate the SVX4 readout chip will have lower noise than the SVX3D chip used in Run IIa. For moderate to high signal-to-noise ratios and readout pitches less than $\sim$ 200 μm, intermediate strips provide better resolution with relatively little loss of two-track separation relative to sensors with the same readout pitch and no intermediate strips.

A full hit-level simulation from the Run IIb tracking system was not available to guide the design of the detector we propose to build for Run IIb. The data from Run IIa is just becoming available and the tracking (particularly in the stereo view) is in an early stage of development. Consequently, we embarked on a program of evaluating our design with a number of targeted studies along with, when available, information from the data.

The remaining portions of this chapter describe studies of the impact parameter resolution (4.2), the